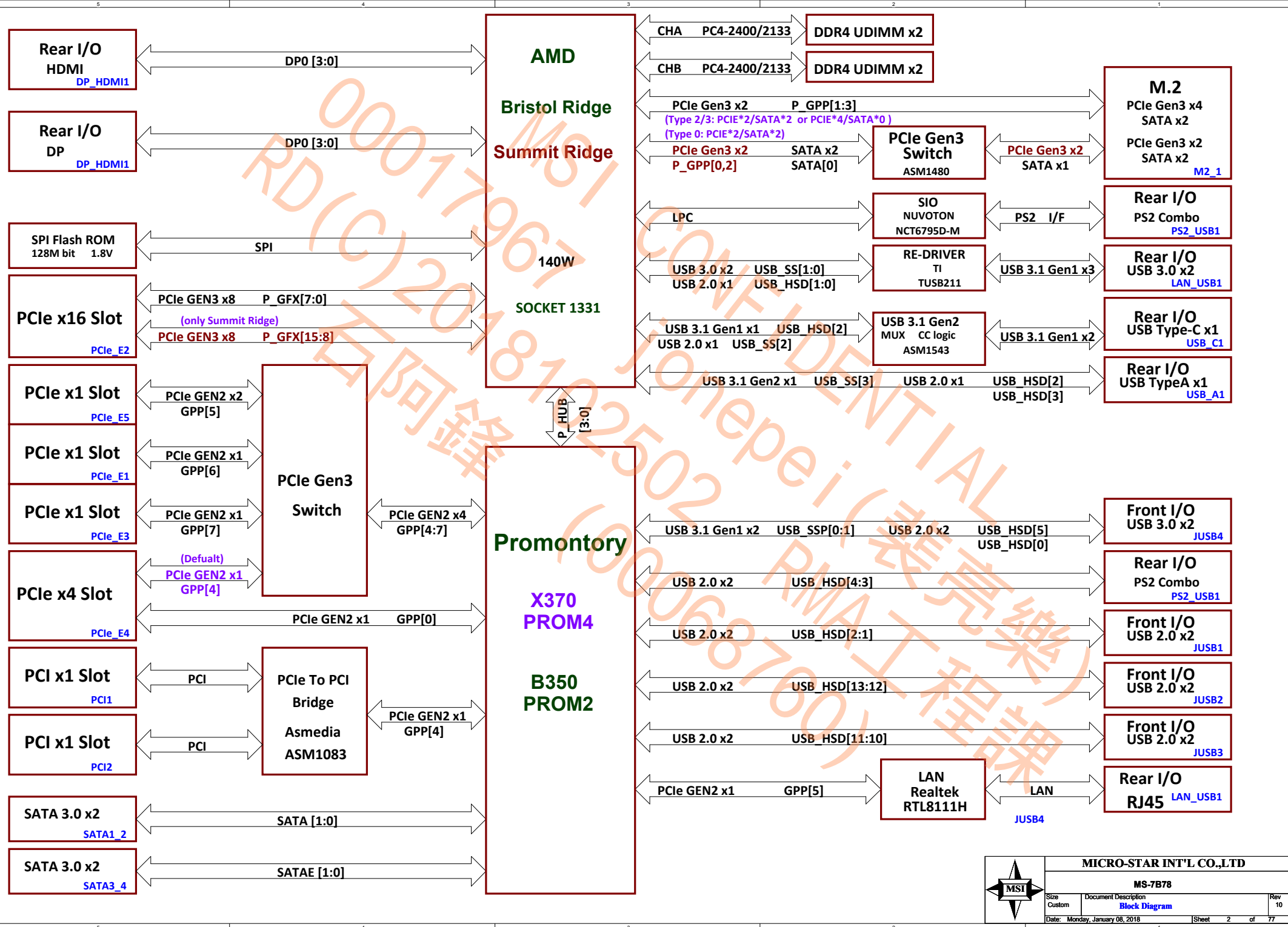
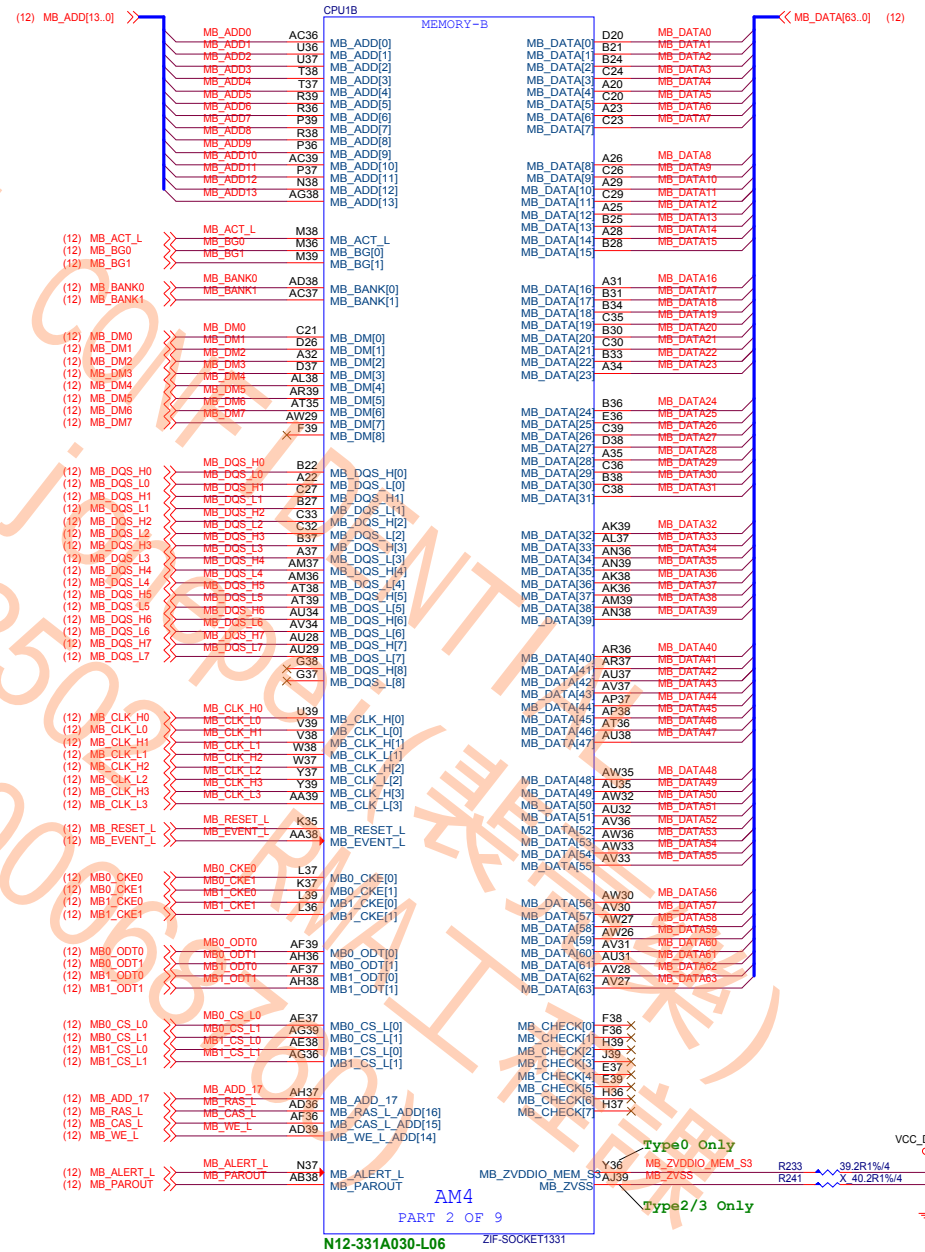


# AMD AM4

01	Cover Sheet	36	LAN - I211AT	66	MCU - LED Control
02	Block Diagram	37	Audio ALC1220P-VB	67	LED - Power / JPIPE
03	FM4 DDR4 I / F	38	Audio DePop	68	LED - JLED1 / 2 / 3 / 4
04	AM4 PCIE / SATAE	39	USB Power - UP7501	69	LED - Mystic Light - 1
05	AM4 Display / Audio	40	Front USB2.0 Header	70	LED - Mystic Light - 2
06	AM4 SVI / ACPI / GPIO	41	Front USB3.0 Header	71	BOM Option
07	AM4 LPC / SPI / USB / CLK / STRAP	42	Rear USB3.0 + PS2	72	Manual Parts
08-09	AM4 Power / VDDIO_AUDIO Power / GND	43	Rear USB3.0	73	PG MAP
10	RTC / CMOS	44	Rear USB3.1 Type A / redrive	74	GPIO MAP
11-14	DDR4 - POWER / GND	45	Rear USB3.1 Type A / mux	75	Power Sequence
15	Promontory - PCIE / SATA / SATAE	46	DP	76	Power Delivery
16	Promontory - USB / OC	47	HDMI	77	History
17	Promontory - CLK / ACPI / GPIO	48	CPU power UP9505 10+2		
18-19	Promontory - Power / GND	49	CPU power Phase 1-4		
20	PCI_E2 (X16)	50	CPU power Phase 5-10		
21	PCI_E4 (X8)	51	CPU power NB 1-2		
22	PCIE Switch X16 / X8	52	CPU power NB_S5		
23	PCI_E1_E3_E5 (X1)	53	CPU power 1.8_S0 / S5		
24	PCI_E6 (X4)	54	CPU power VDDP - TPS56C215		
25	PCIE Switch X4 / M2_2	55	VRM PWRGD		
26	M.2_1	56	DDR Power - RT8125E		
27	M.2_2	57	DDR Power - VPP25 / VTT		
28	M.2_3 (WIFI+BT)	58	PROM - SY8288RAC / 1.05V		
29	SIO NCT6797D-M	59	PROM - GS7133 / 2.5V		
30	SIO HW Monitor / NCT7718W	60	OV Control - NCT3933		
31	FAN TYPE-J CPUFAN1	61	OV 12VIN - RT9553B		
32	FAN TYPE-J PUMPFAN1	62	ACPI - 3VSB / 5VDIMM		
33	FAN TYPE-K SYSFAN1/2	63	ATX Power - FrpntPanel / EMI		
34	FAN TYPE-K SYSFAN3/4	64	LED - EZDEBUG / AMP		
35	FAN GPIO NCT5605	65	LED - DIMM / PCIE SLOT		

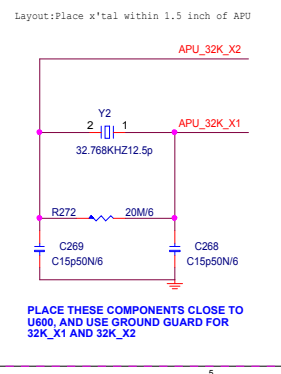
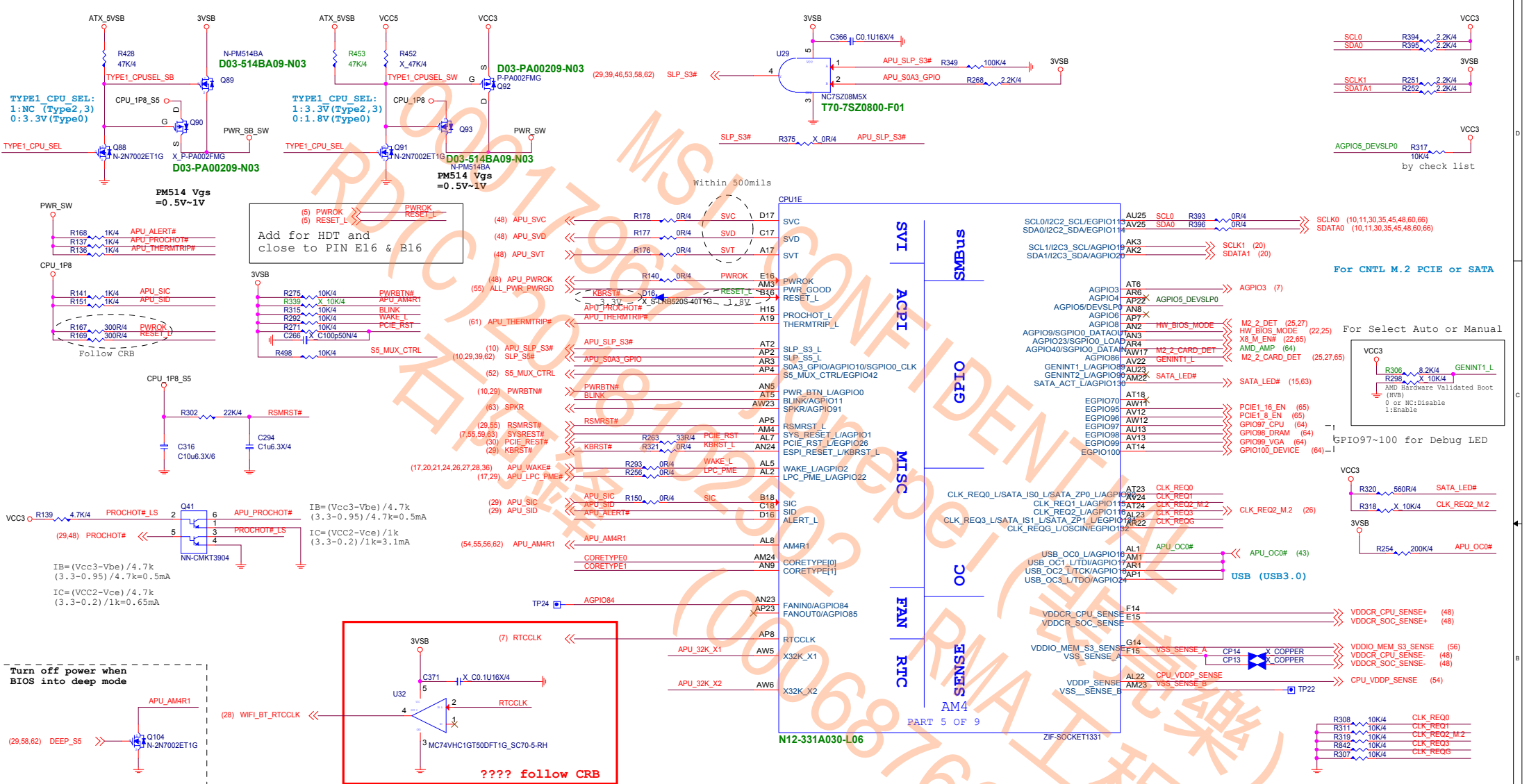




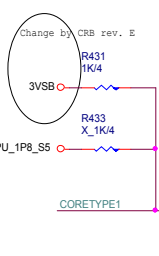








### AM4 CPU TYPE Circuit



CPU	TYPE	CORETYPE0	CORETYPE1
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1

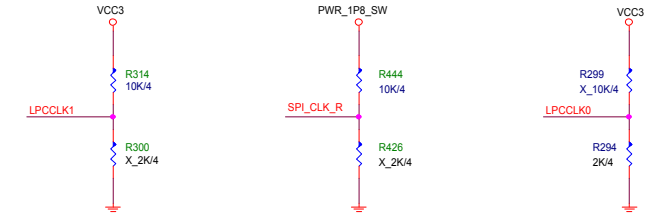
TYPE1\_CPU\_SEL (5.43,52,54,55)  
TYPE1\_CPU\_SEL  
0:BR/NA  
1:ST/RV/ZP  
IB=(Vcc3-Vbe)/21k  
(3.3-0.95)/21k=0.111mA  
IC=(VCC5-Vce)/10k  
(5-0.2)/47k=0.102mA

IB=(CPU\_1P8\_S5-Vbe)/5.7k  
(1.8-0.95)/5.7k=0.149mA  
IC=(VCC5-Vce)/47k  
(5-0.2)/47k=0.102mA

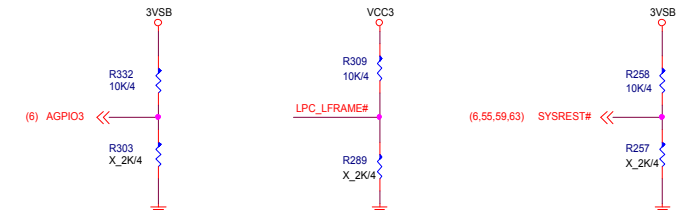
**MICRO-STAR INT'L CO.,LTD**  
**MS-7B78**

Size Custom	Document Description <b>AM4 SV1/ACPI/GPIO</b>	Rev 10
Date: Tuesday, January 09, 2018		Sheet 6 of 77

# Strapping Options

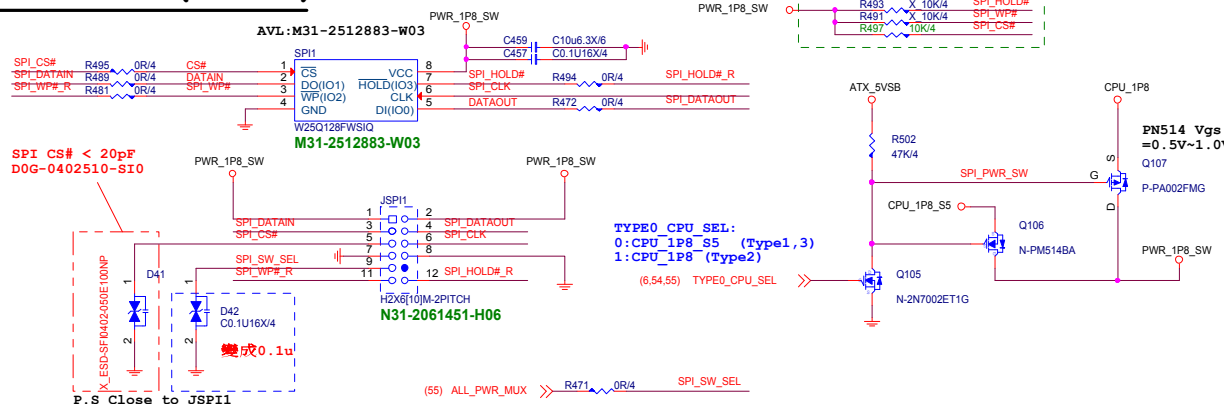


	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	LPC device Boot Fail Timer Enabled
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIe clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled (Default)

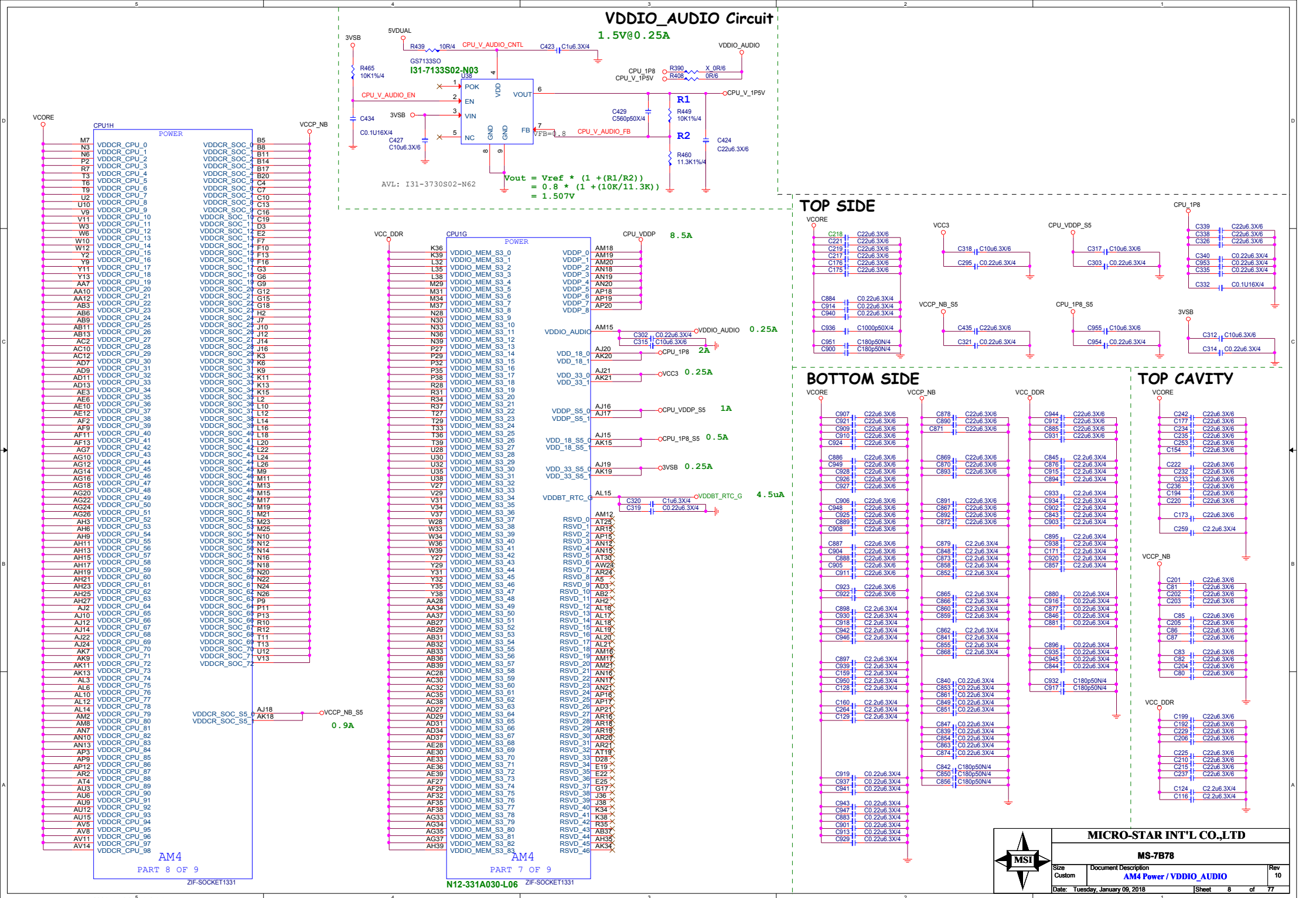


	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

## SPI ROM(1.8V)



MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size Custom	Document Description	Rev 10
AM4 LPC / SPI / USB / CLK / STRAP		
Date: Tuesday, January 09, 2018	Sheet 7	of 77

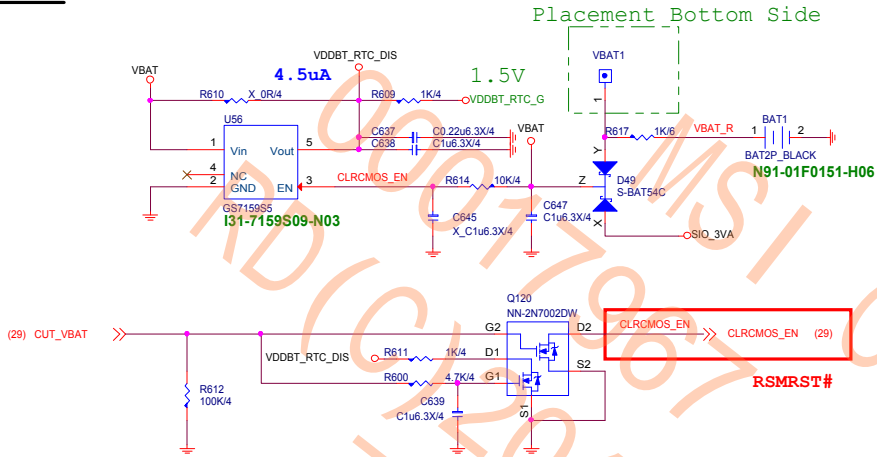




GND

AM4  
PART 9 OF 9

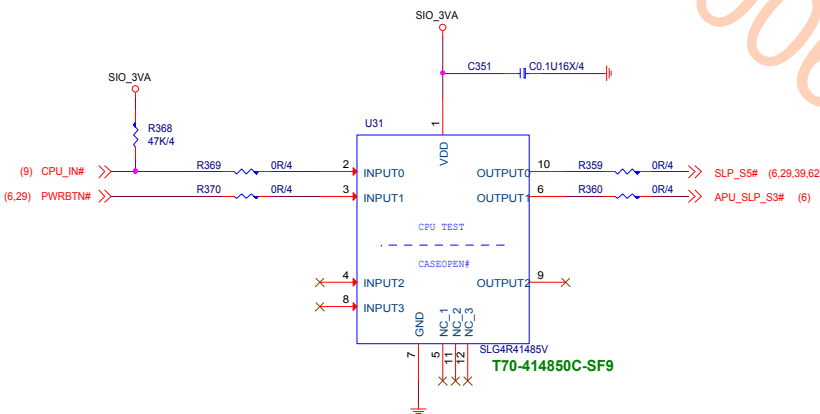
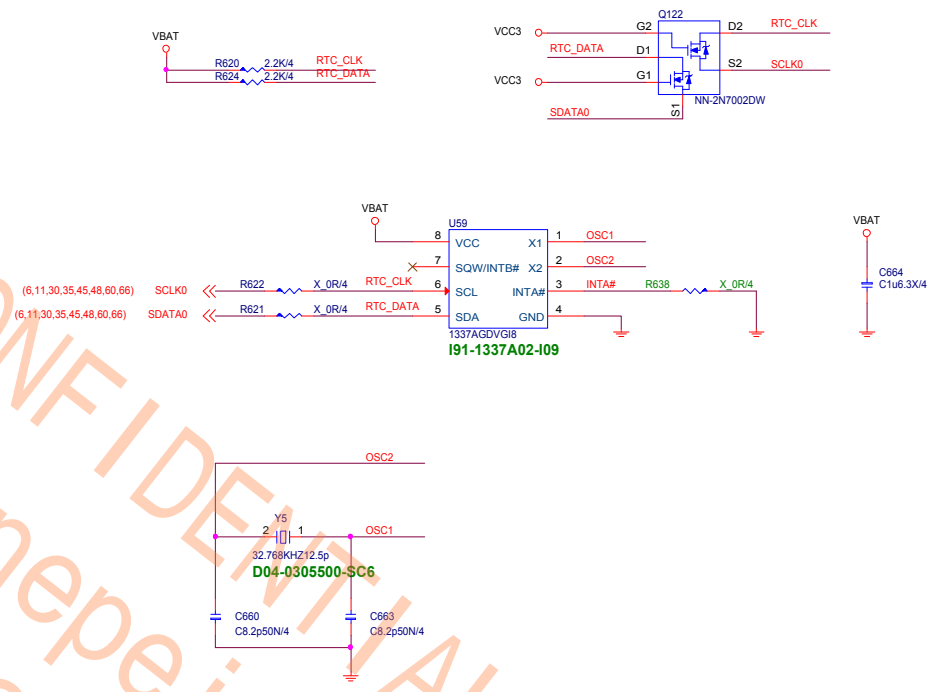
RTC & Clear CMOS Circuit

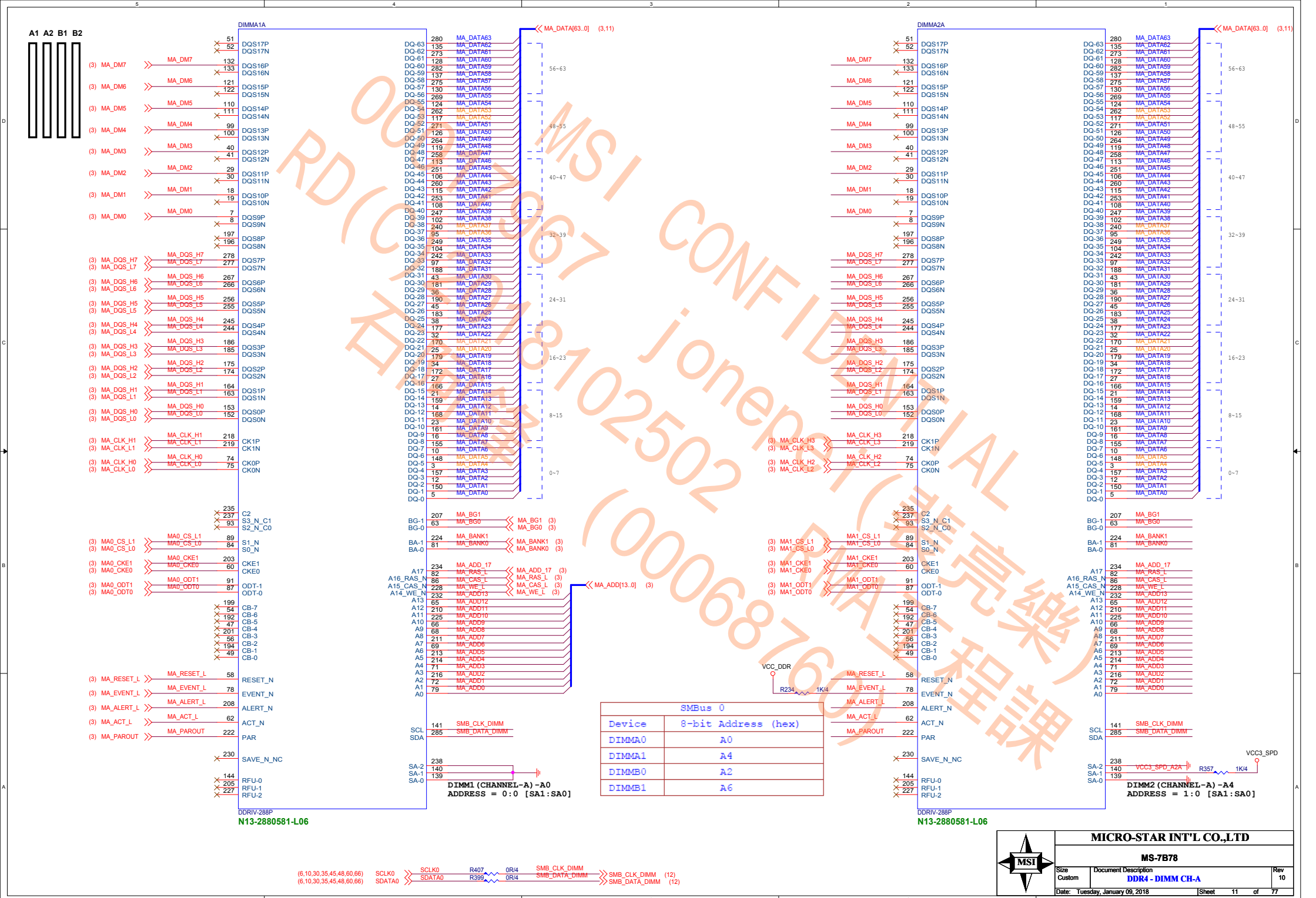


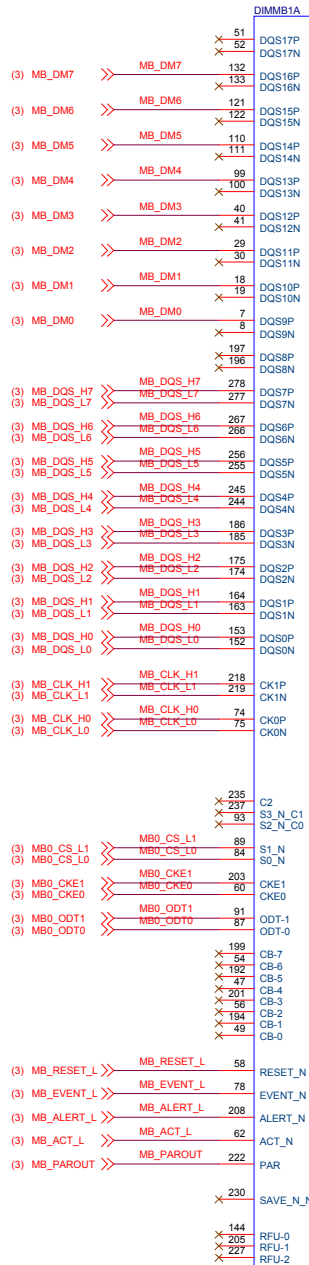
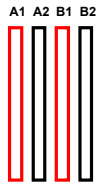
Clear CMOS button



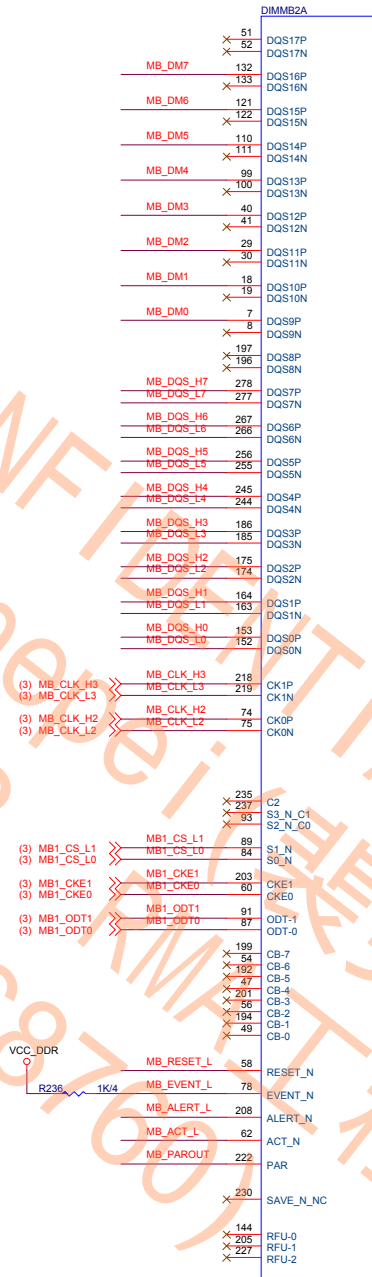
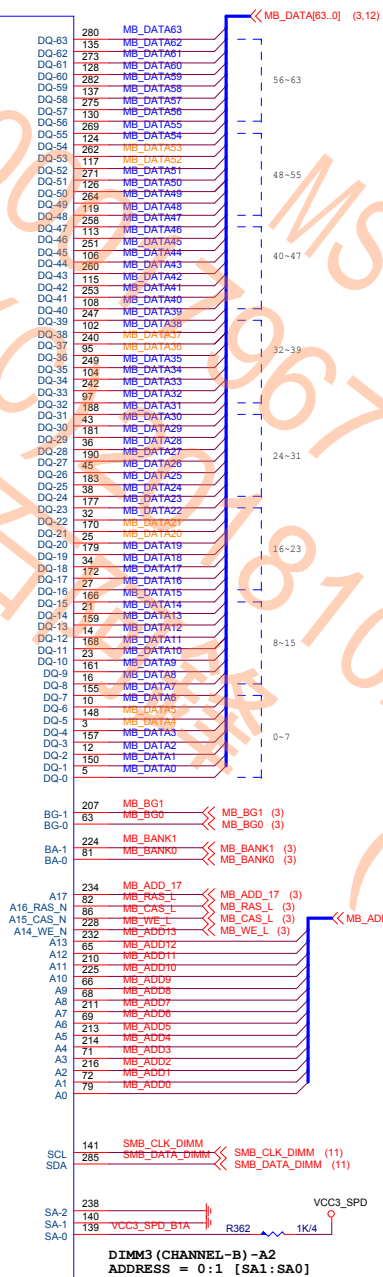
RTC Backup







DDRIV-288P  
N13-2880581-L06



DDRIV-288P  
N13-2880581-L06



MICRO-STAR INT'L CO.,LTD

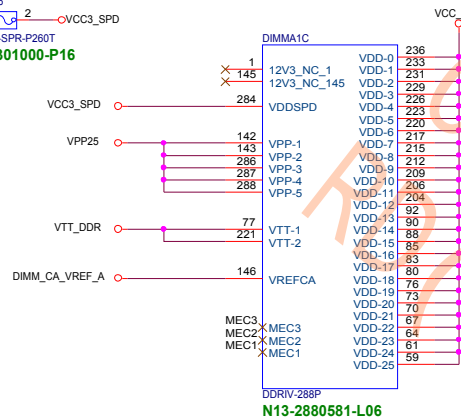
MS-7B78

Size	Document Description	Rev
Custom	DDR4 - DIMM CH-B	10
Date: Tuesday, January 09, 2018		Sheet 12 of 77

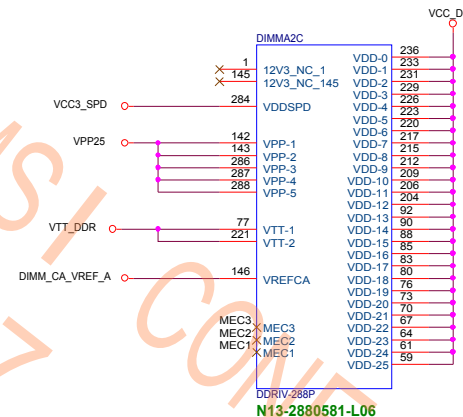
av1:D08-0301100-B07

VCC3 SPD  
F8  
F-SPR-P280T  
VCC3 SPD

D08-0301000-P16

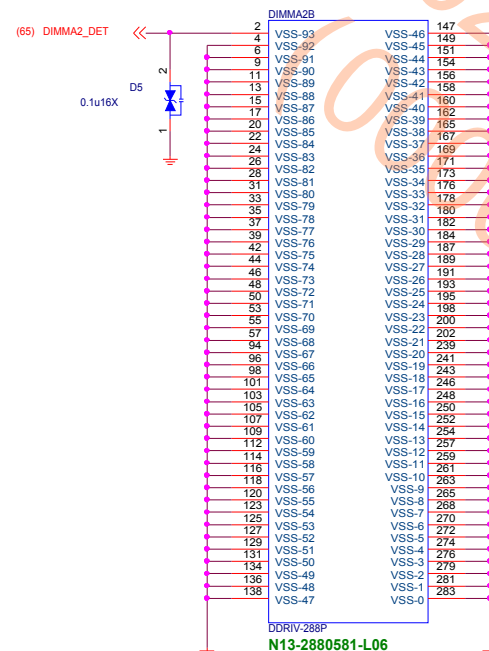
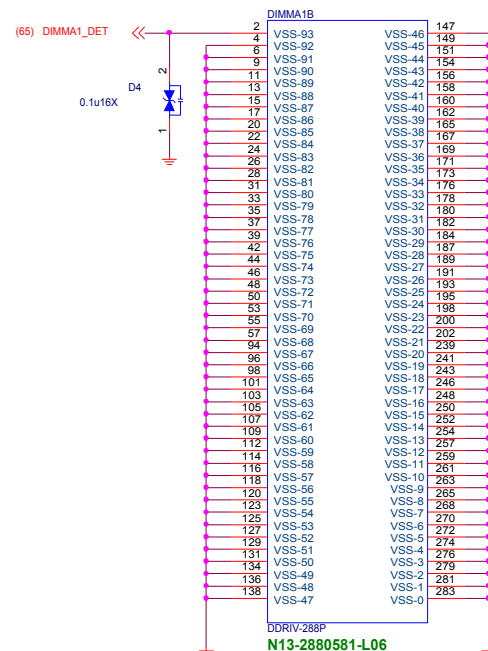
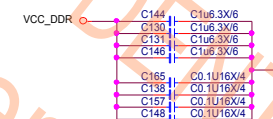
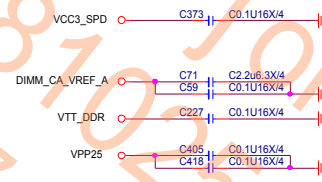
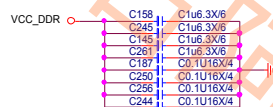
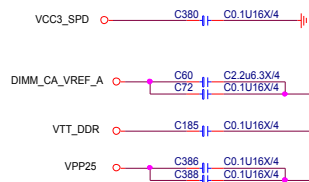
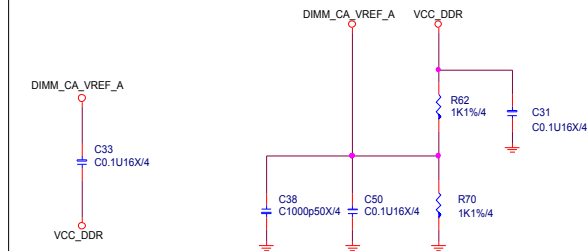


DIMM SLOT PN BY SPEC



## DDR VREF

(place resistors close to DIMMs)



MICRO-STAR INT'L CO.,LTD

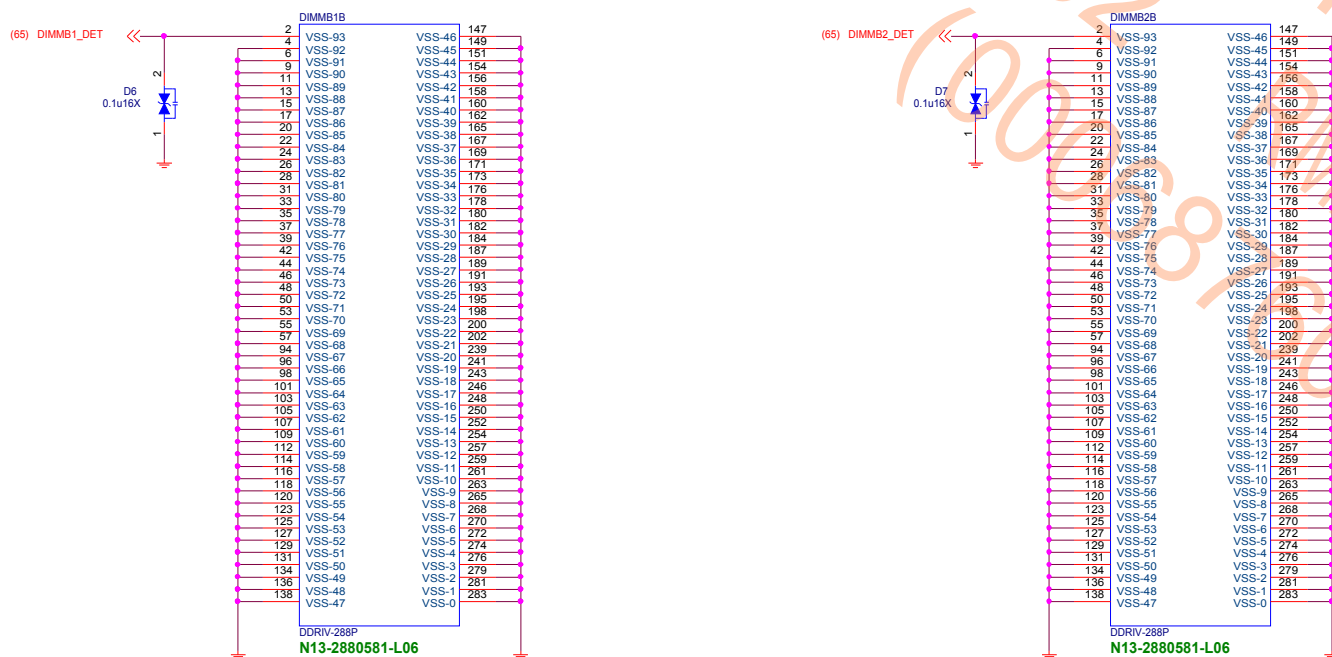
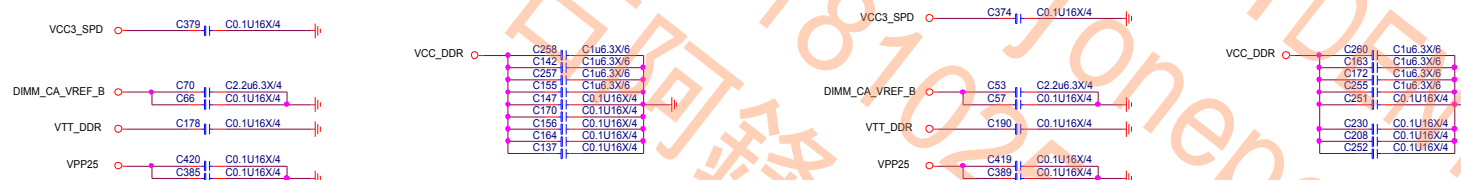
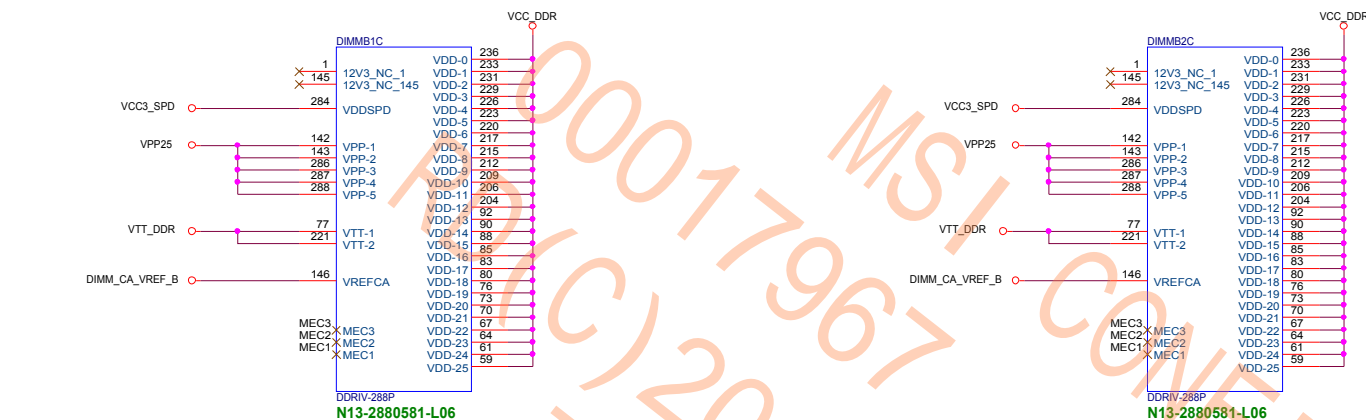
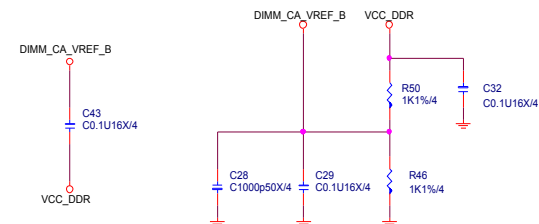
MS-7B78

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	10
Date: Tuesday, January 06, 2016	Sheet 13 of 77	



# DDR VREF

(place resistors close to DIMMs)



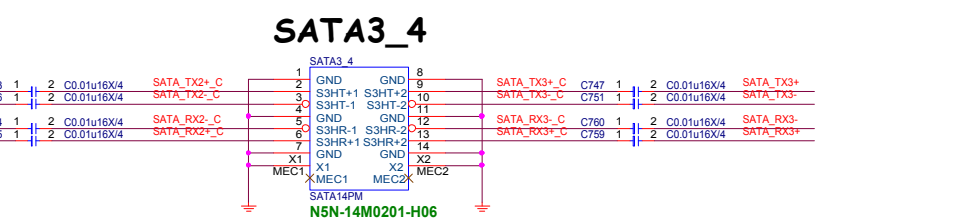
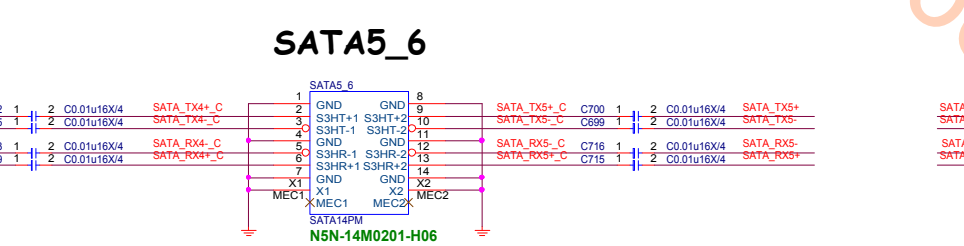
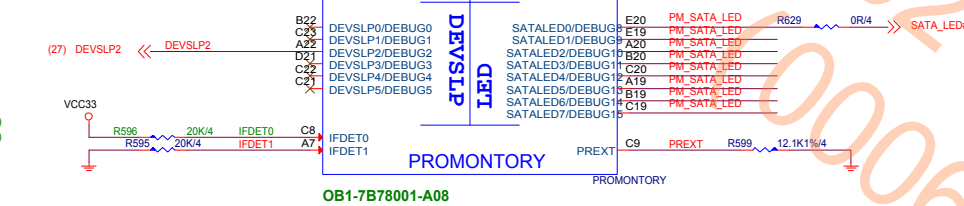
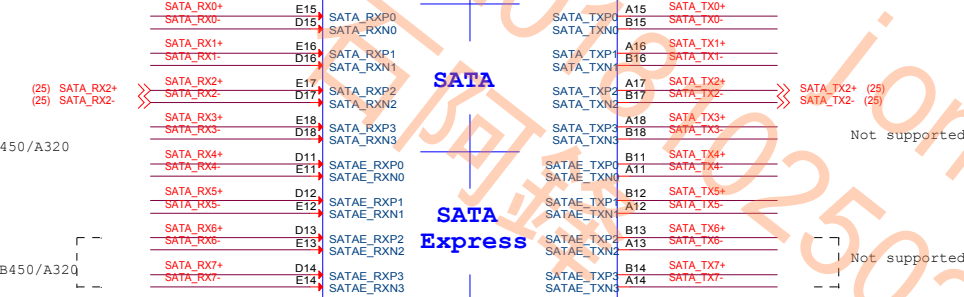
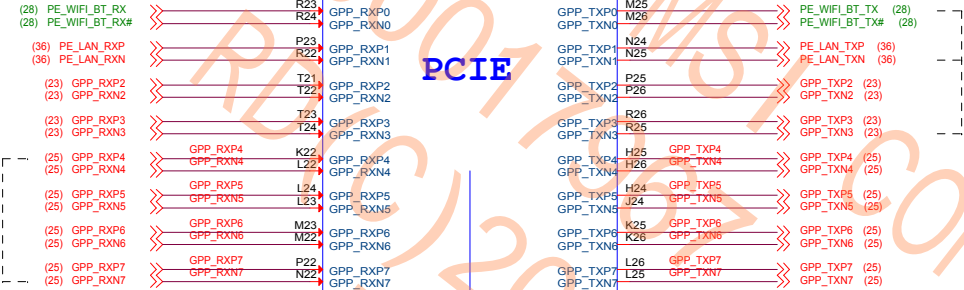
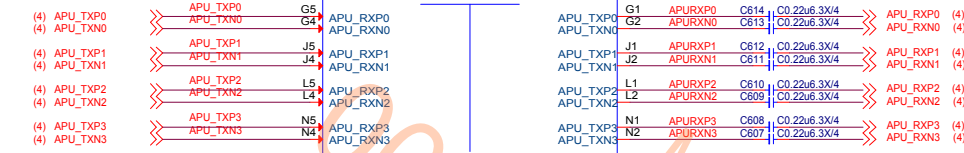
WIFI+BT

LAN

PCI\_E2

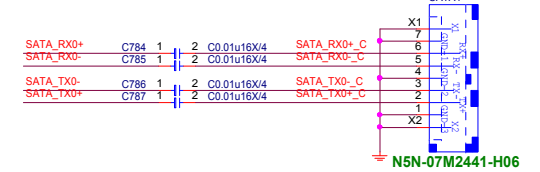
PCI\_E4

PCI\_E5\_M2\_2

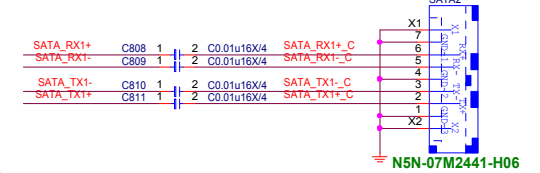


## SATA Connector

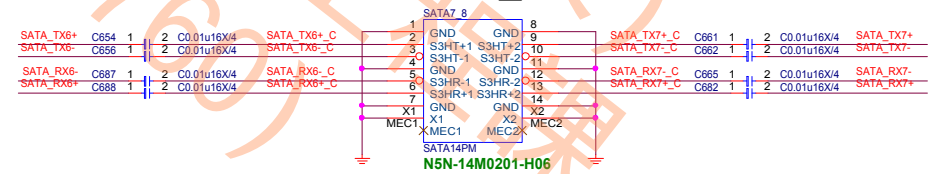
### SATA1



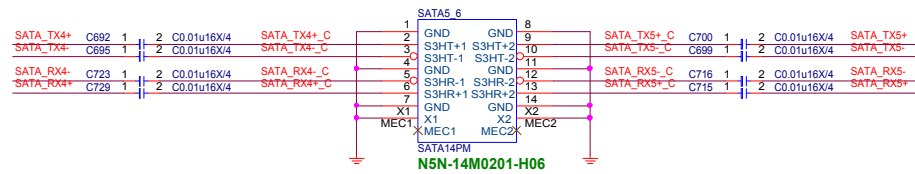
### SATA2



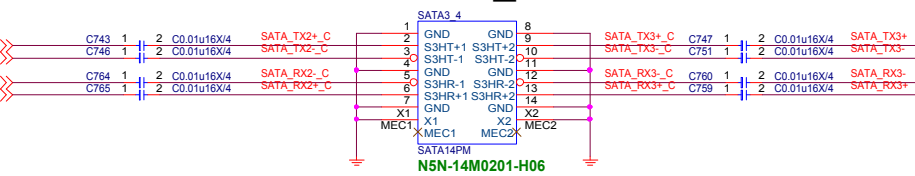
### SATA7\_8



### SATA5\_6



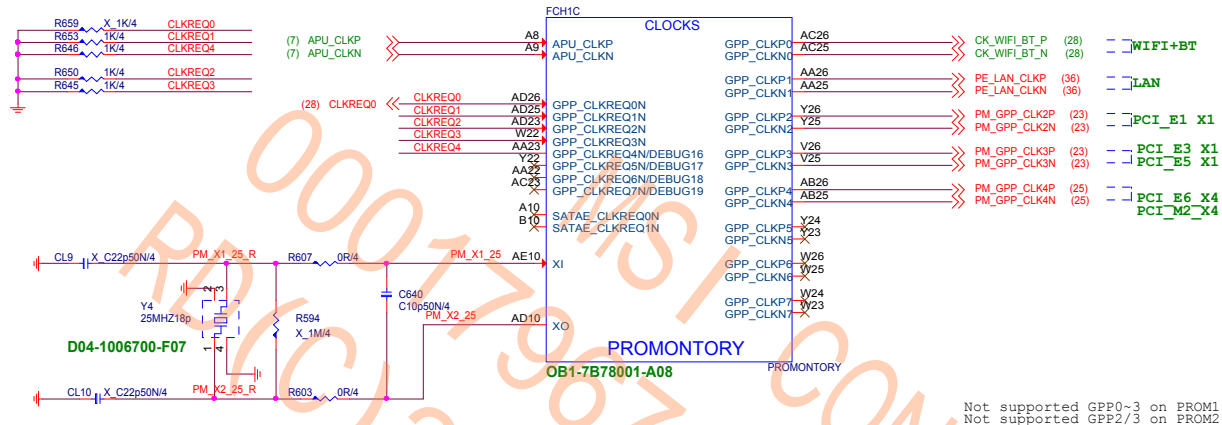
### SATA3\_4



MICRO-STAR INT'L CO.,LTD			
MS-7B78			
Size	Document Description	Rev	
Custom	Promontory - PCIE/SATA/SATAE	10	
Date:	Tuesday, January 09, 2018	Sheet	15 of 77



GPP Clock	CLKREQ#
GPP_CLKP/N[0]	GPP_CLKREQ0N
GPP_CLKP/N[1]	GPP_CLKREQ1N
GPP_CLKP/N[2]	GPP_CLKREQ2N
GPP_CLKP/N[3]	GPP_CLKREQ3N
GPP_CLKP/N[4]	GPP_CLKREQ4N
GPP_CLKP/N[5]	GPP_CLKREQ5N
GPP_CLKP/N[6]	GPP_CLKREQ6N
GPP_CLKP/N[7]	GPP_CLKREQ7N



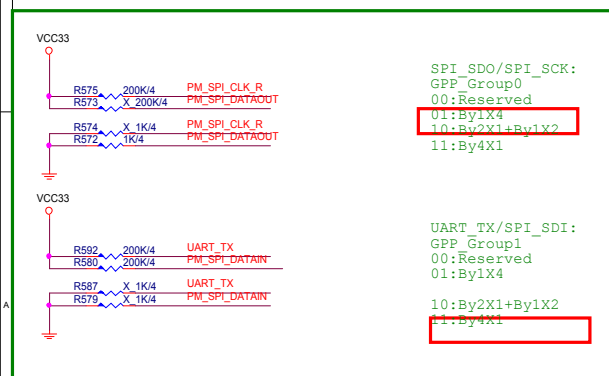
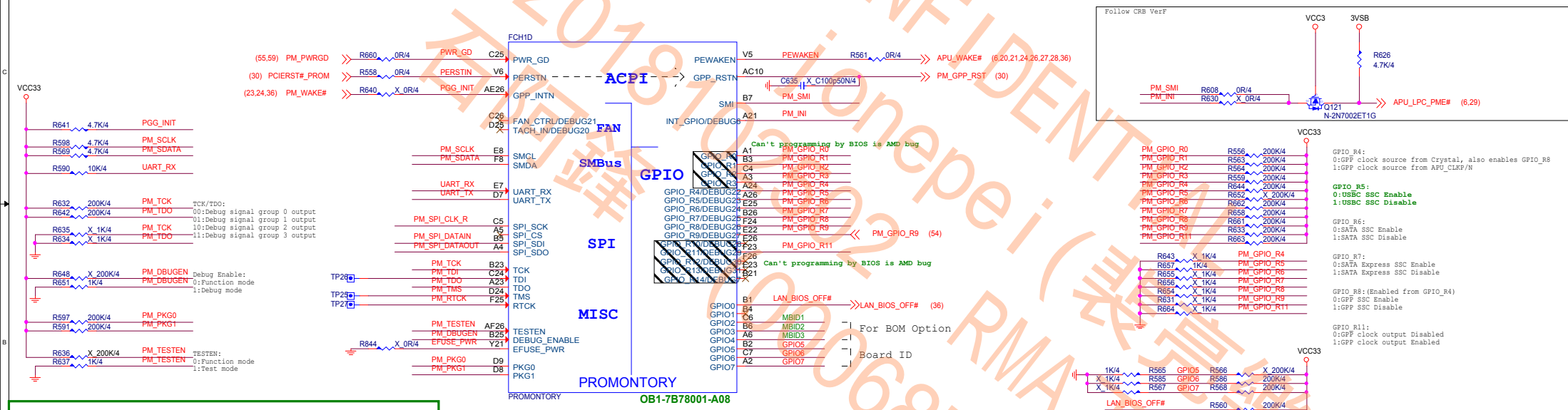
Not supported GPP0~3 on PROM1  
Not supported GPP2/3 on PROM2

## Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0-1	USB_SS Port 0-5	USB_HSD Port0-13 USB_HSD Port10-13	USB_SSP Port
PROM2	USB_SSP Port0-1	USB_SS Port 0-1	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port
PROM1	USB_SSP Port0	USB_SS Port USB_SSP Port	USB_HSD Port0-5 USB_HSD Port10, 12-13	USB_SSP Port

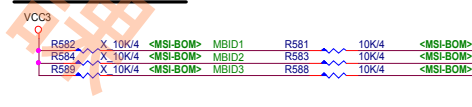
BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
FROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
FROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用  
CLK1-3不能用

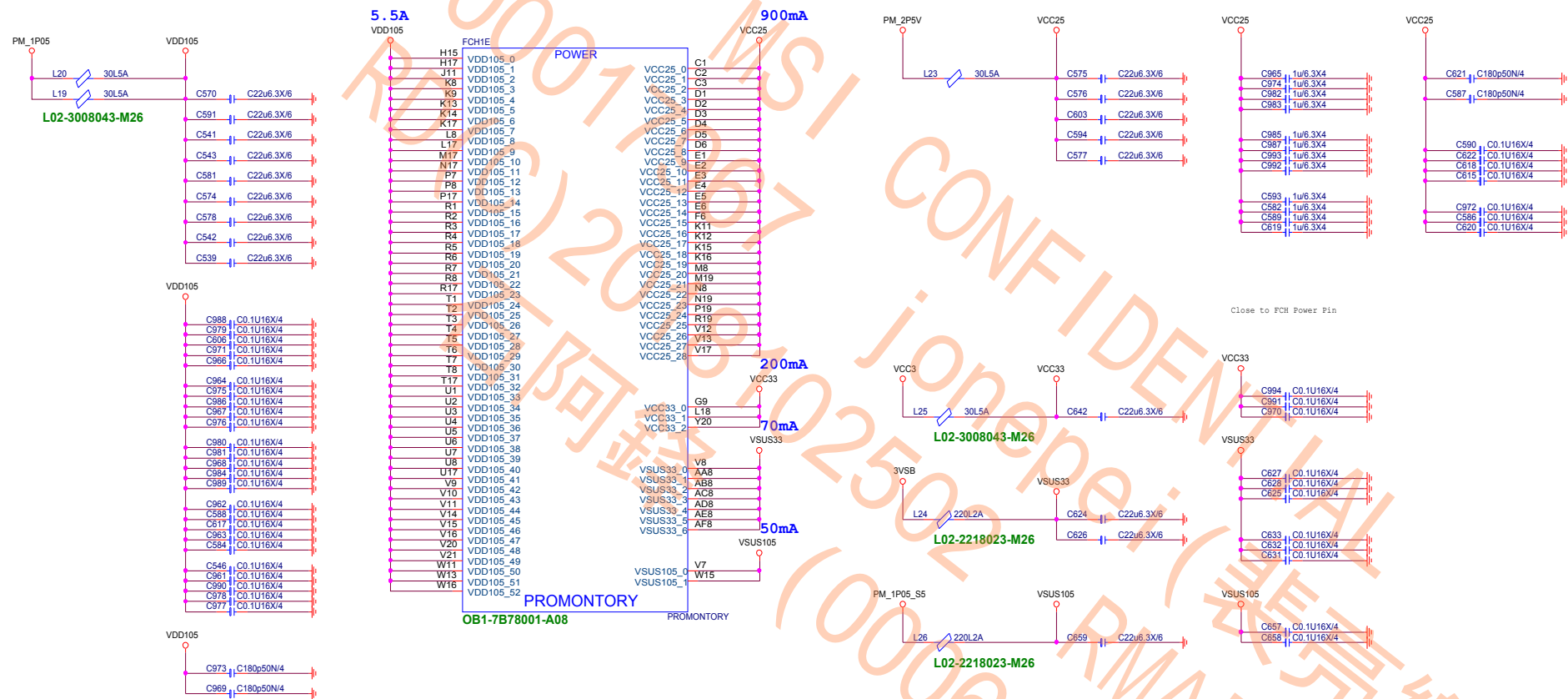


	MBID3	MBID2	MBID1
2470	0	0	0

## BOM OPTION



<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7B78</b>			
Size Custom	Document Description <b>Promontory - CLK/ACPI/GPIO</b>		Rev 10
Date: Tuesday, January 09, 2018	Sheet	17	of 77

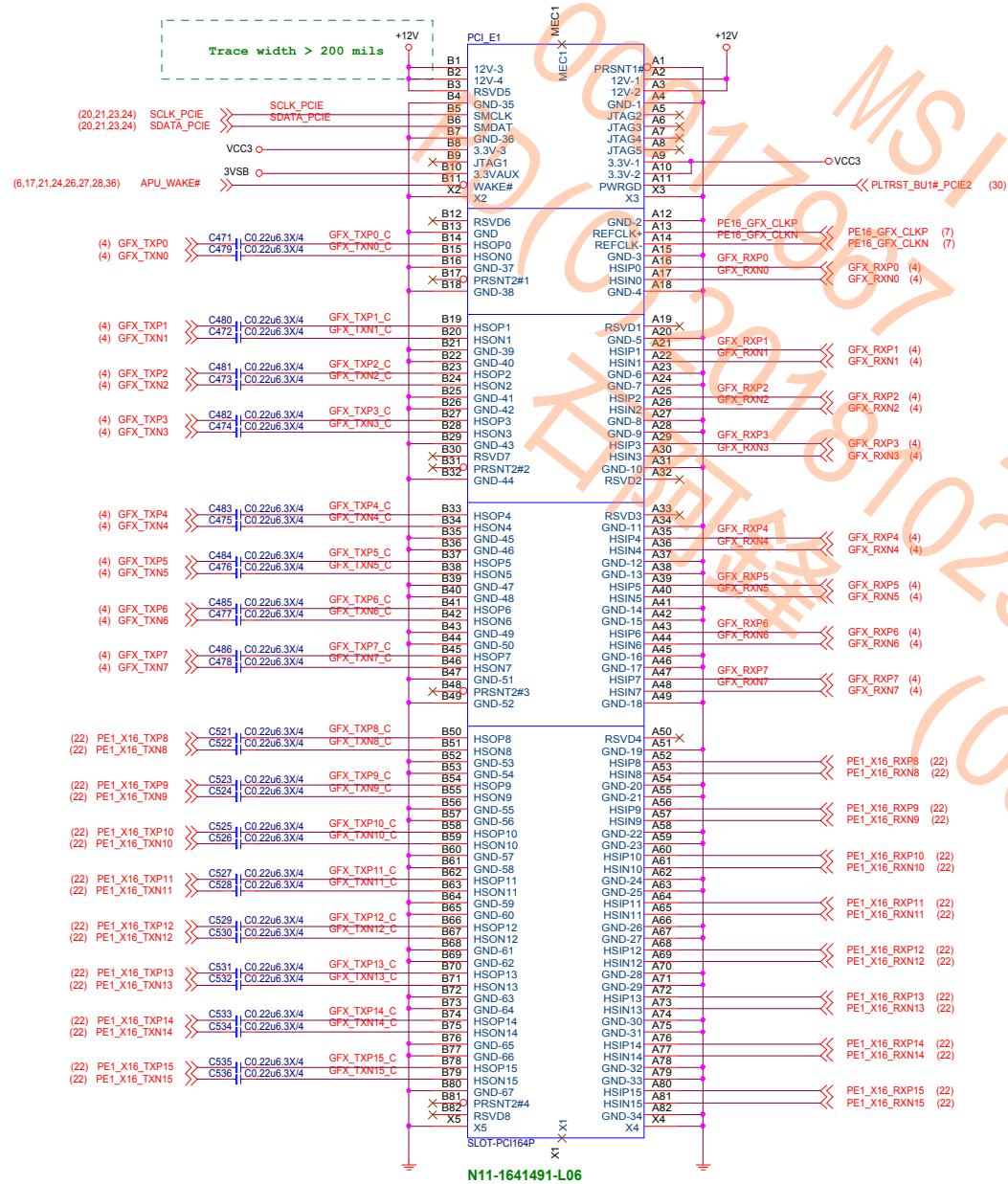




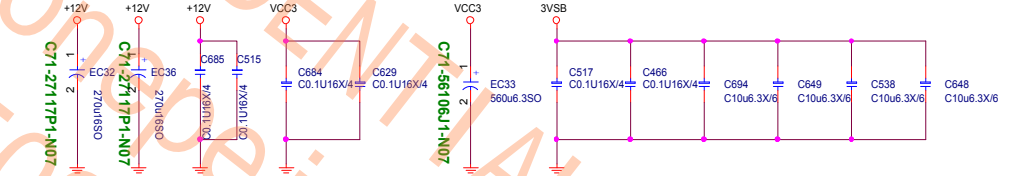
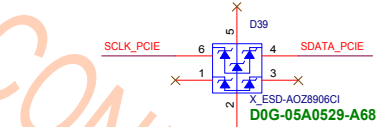
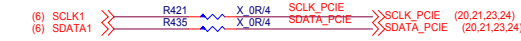


# PCI EXPRESS x16 Slot

## PCI\_E1

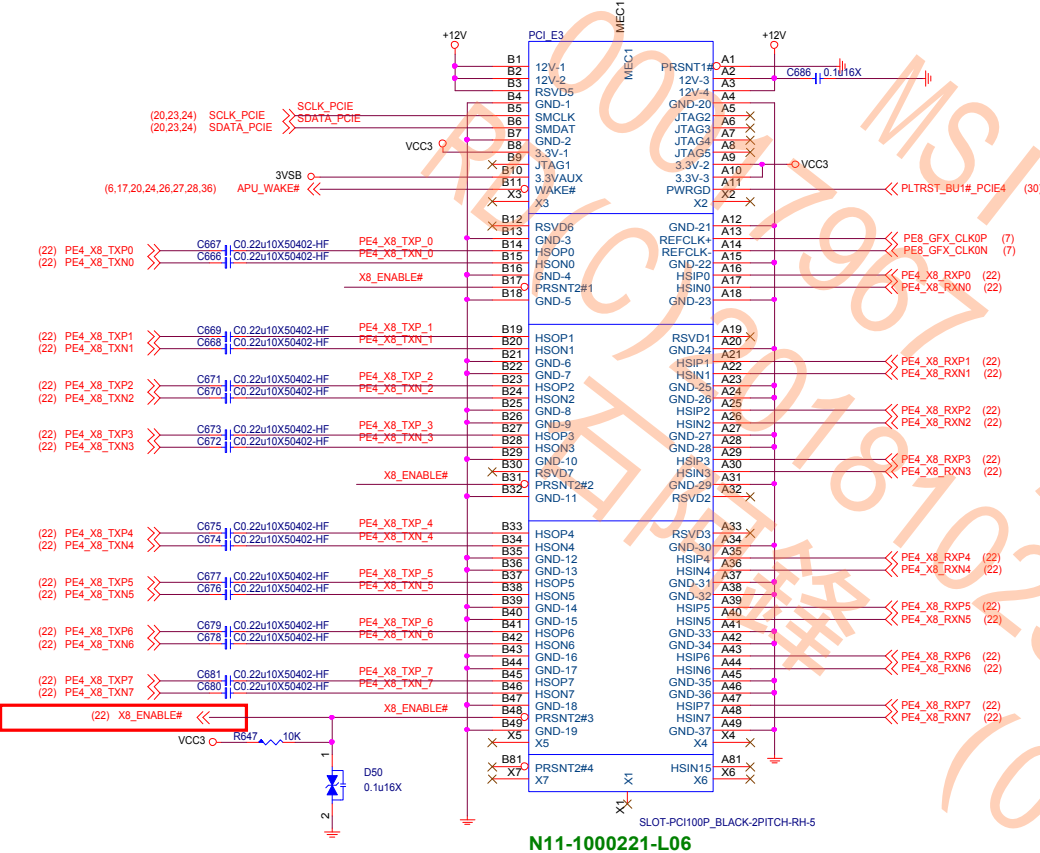


## SMB\_SEL GPIO Default High




PCI EXPRESS x8 SLOT

PCI\_E3



PCI Express x8 Slot		
+12V	-	A
+VCC3	-	3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

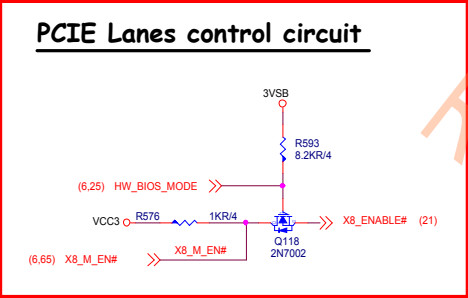


MICRO-STAR INT'L CO.,LTD

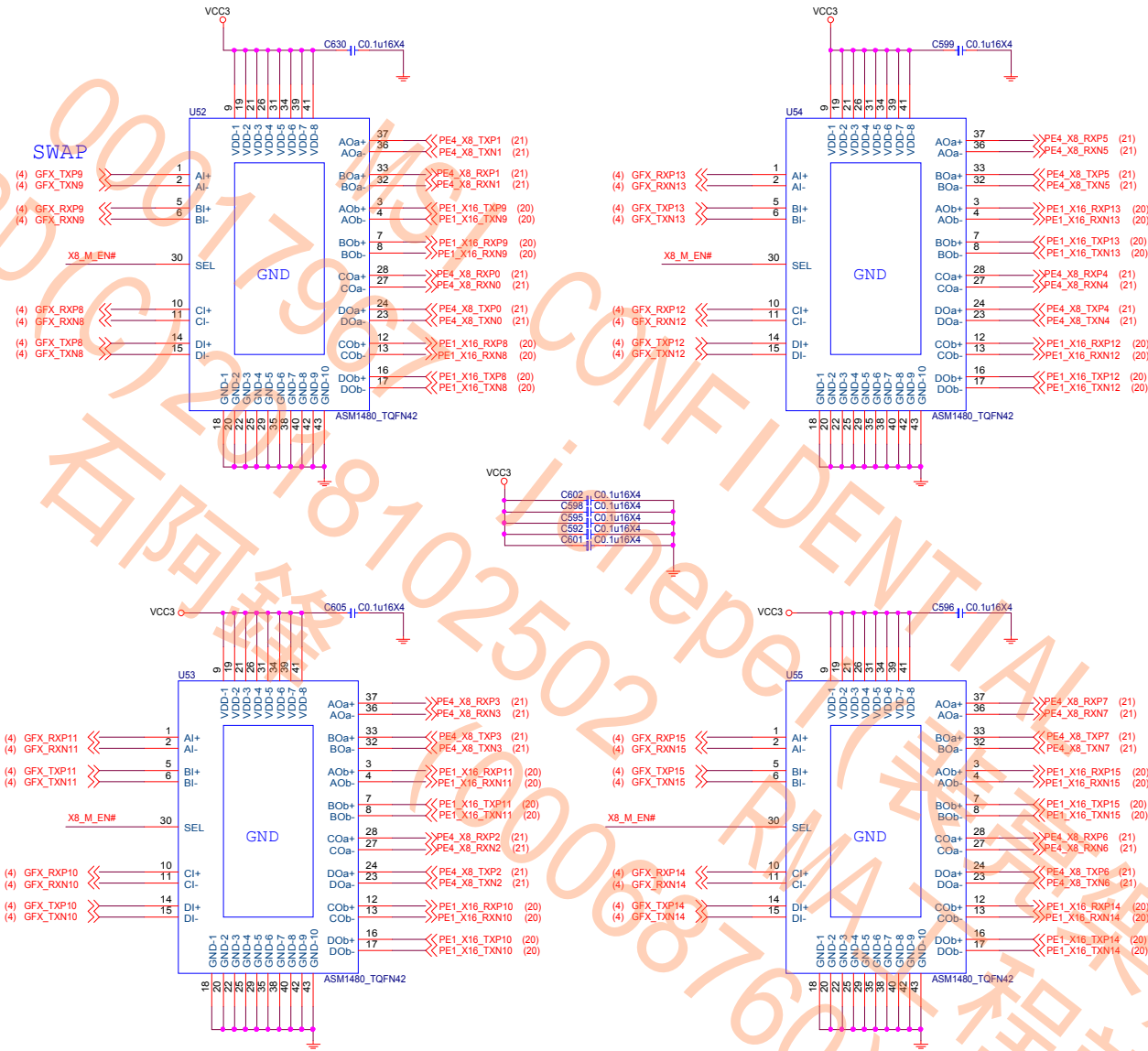
MS-7B78

Size	Document Description	Rev
Custom	PCI_E4 (X8)	10
Date:	Tuesday, January 09, 2018	Sheet 21 of 77

PCI EXPRESS Switch  
For PCIE1 & PCIE3

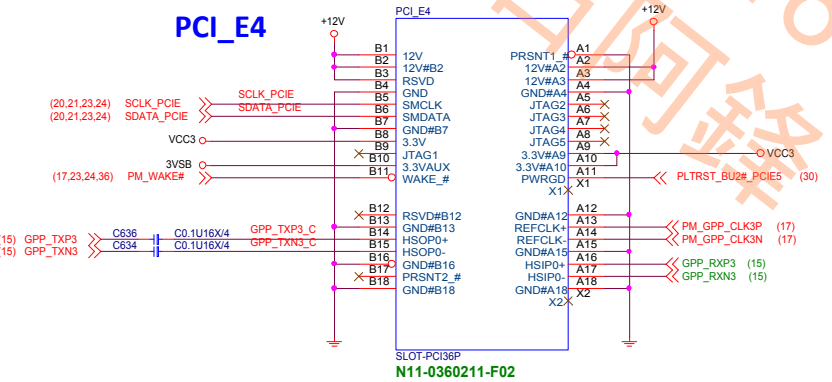
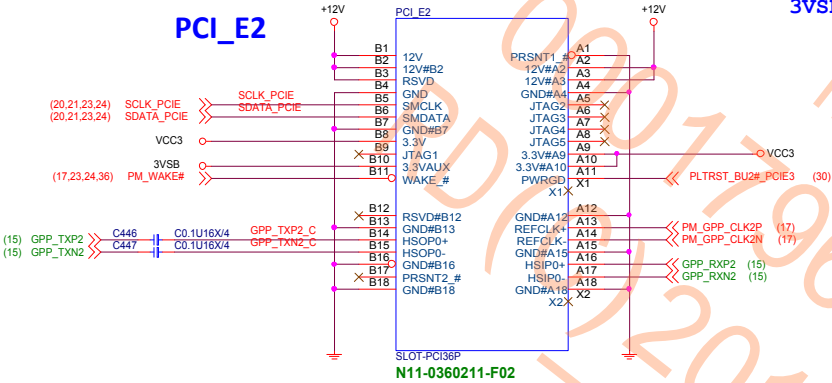


	HW_BIOS_MODE	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0



PCI EXPRESS X1 SLOT

12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



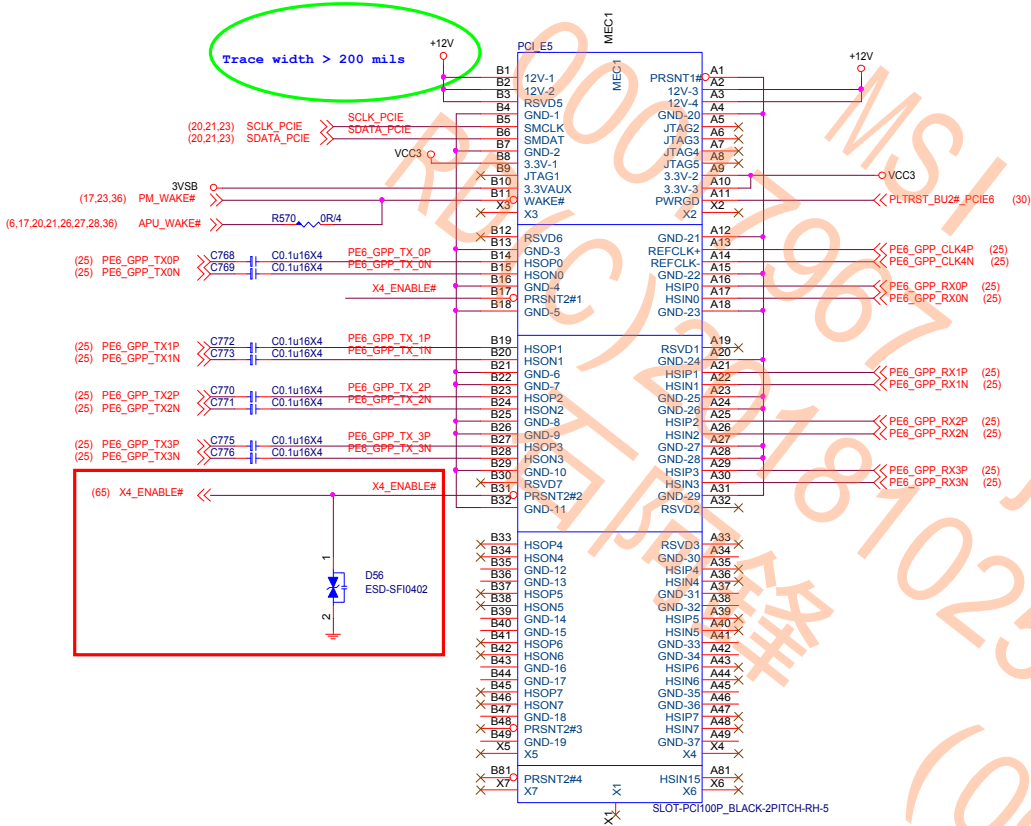
PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA

MICRO-STAR INT'L CO.,LTD			
MS-7B78			
Size	Document Description	Rev	
Custom	PCI_E1_E3_E5(XI)	10	
Date:	Tuesday, January 09, 2018	Sheet	23 of 77




PCI EXPRESS X4 SLOT

PCI\_E6



PCI Express x4 Slot *1	
+12V	- 2.1A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



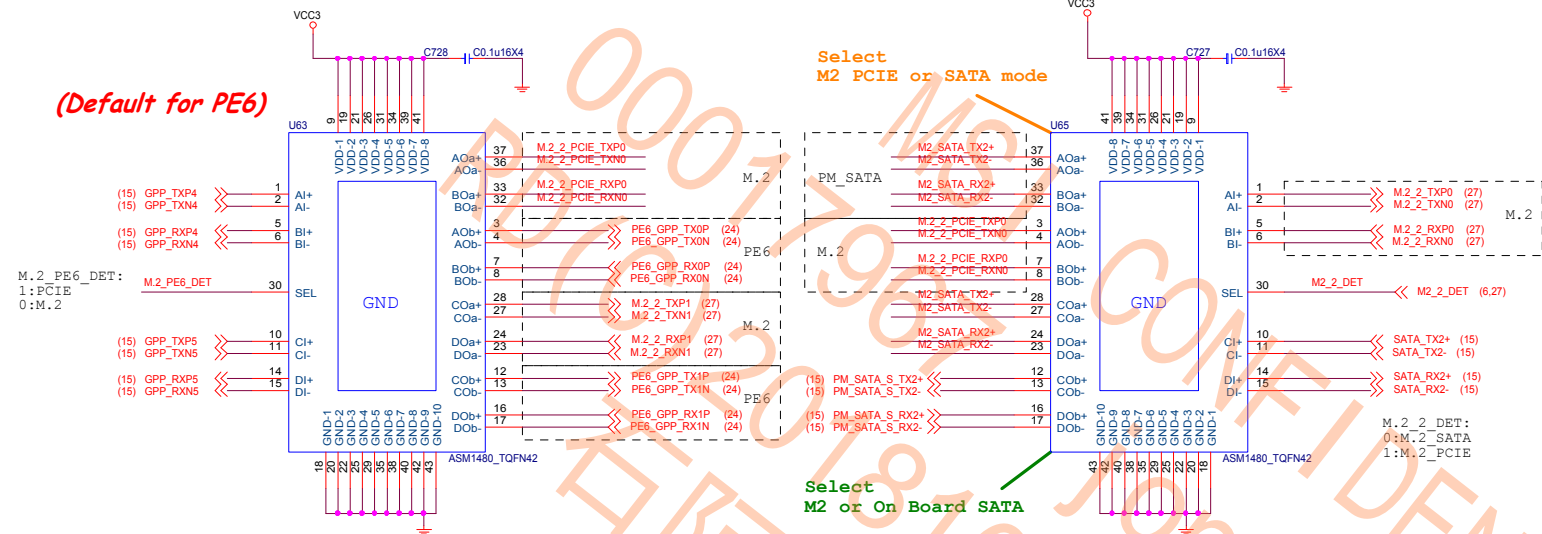
MICRO-STAR INT'L CO.,LTD

MS-7B78

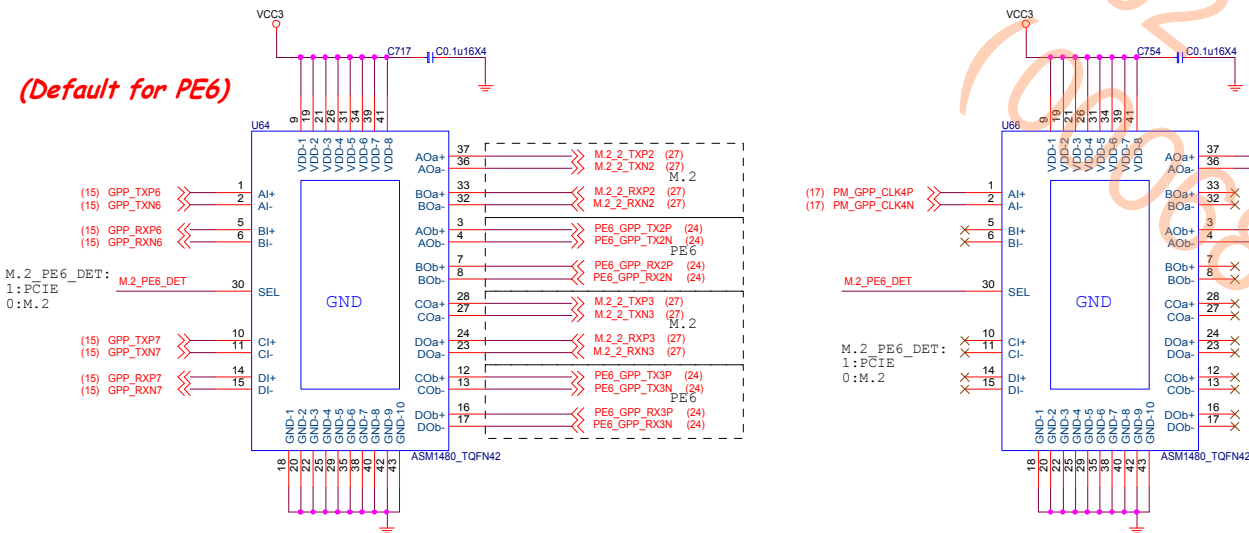
Size Custom	Document Description PCI_E6 (X4)	Rev 10
Date: Tuesday, January 09, 2018	Sheet 24 of 77	

# PCI E6 and M2 2 and SATA1 Switch

(Default for PE6)

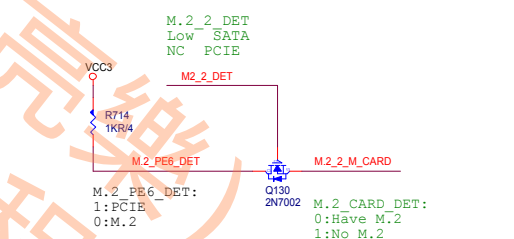
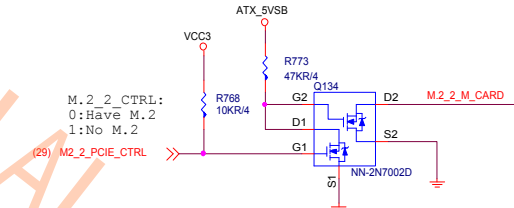
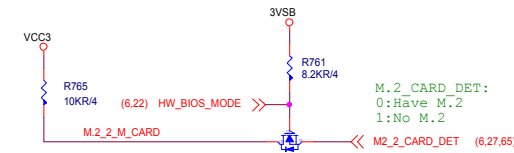


(Default for PE6)



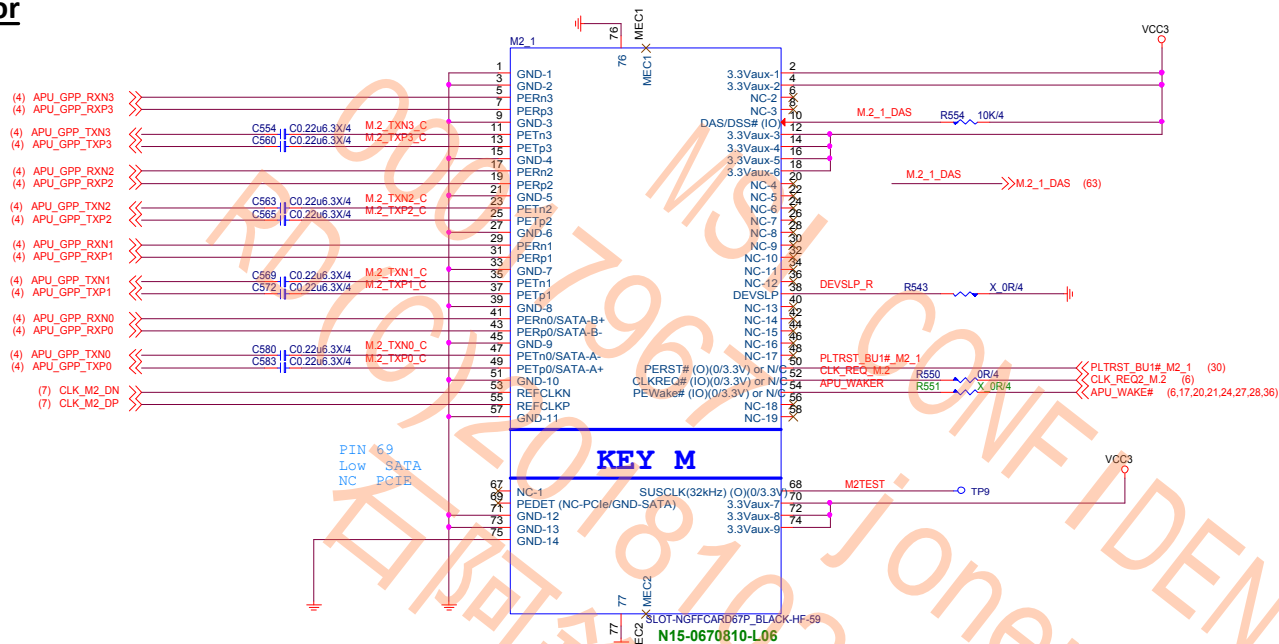
Manufacture Control					
	AUTO Mode	PCIE X4	M.2 X4	M.2 SATA	SATA5
HW_BIOS_MODE	1	0	0	1	
M2_2_PCIE_CTRL	0	1	0	0	
Device Detect					
M2_2_CARD_DET		1	0	0	1
M2_2_DET		1	0	1	0

紅色數字為判抓到PCIE或SATA device時所要判斷的訊號

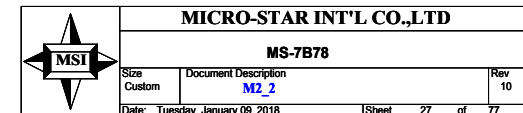


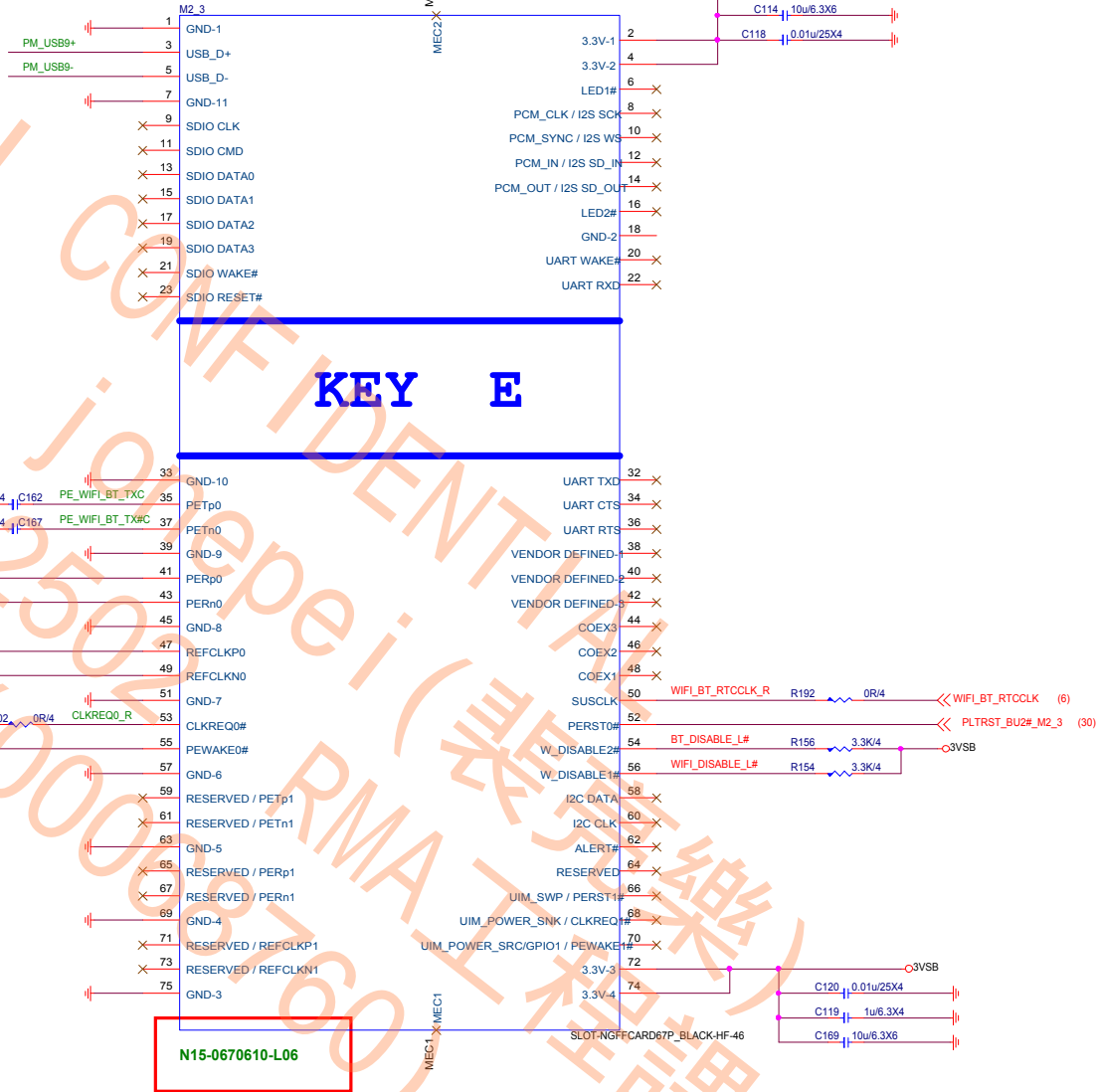
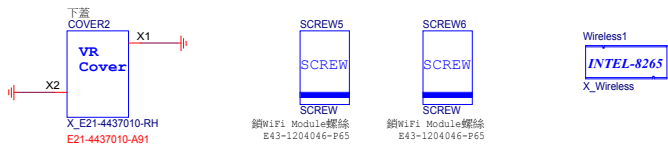
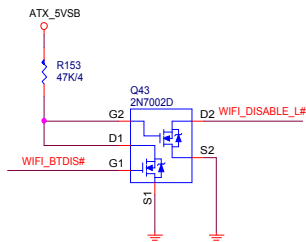
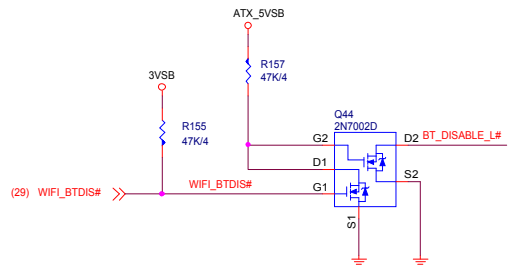
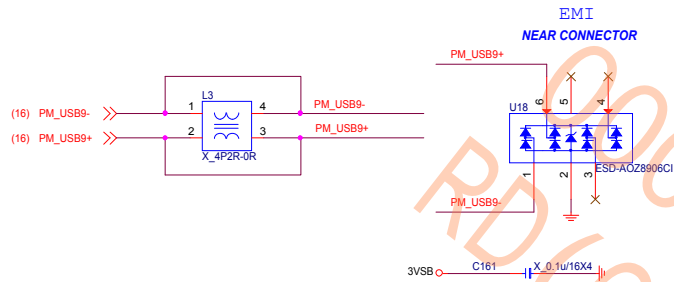
## M.2 1 Connector

3.3V@2.5A



## 3.3V@2.5A

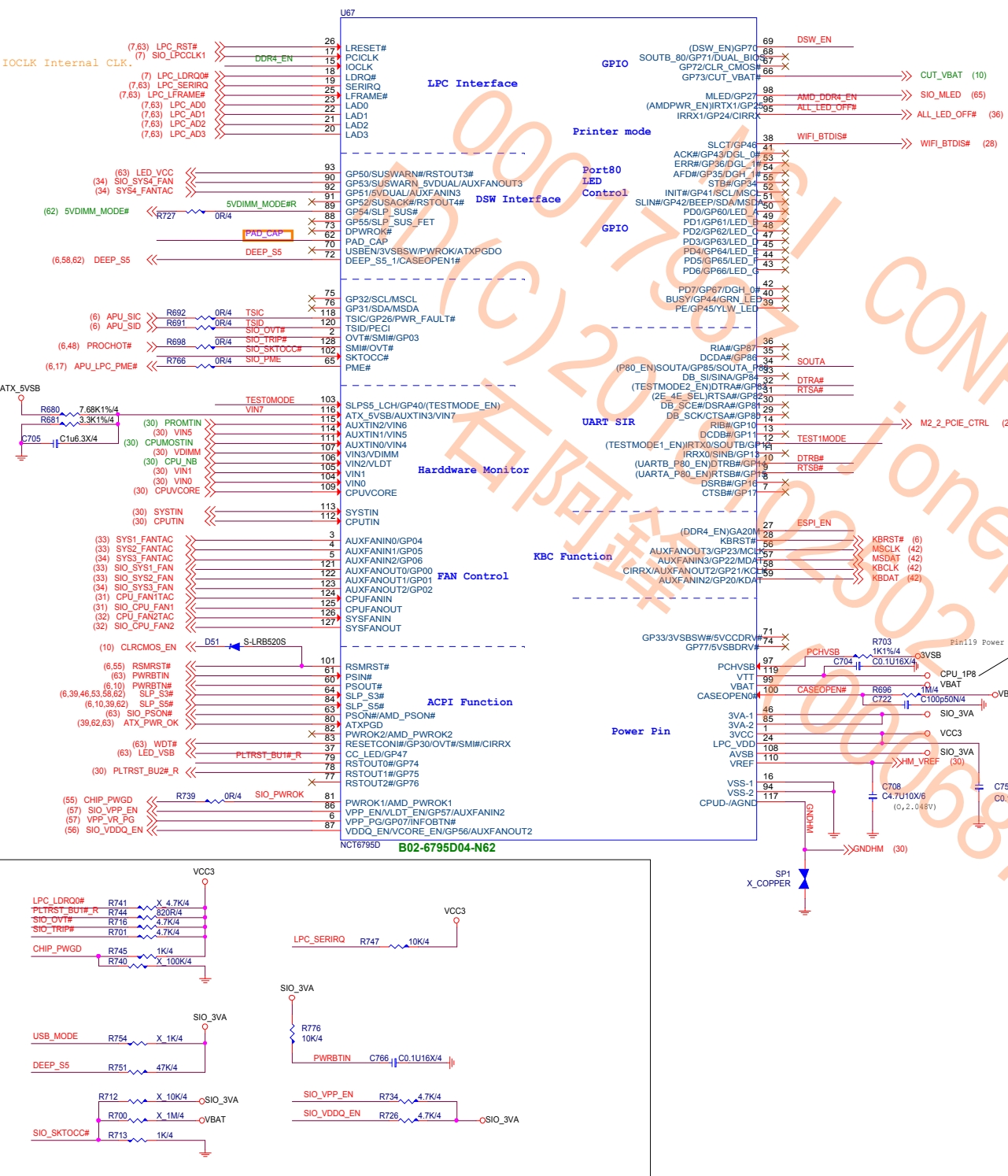




10uP+0.1uP+0.01uP at one end of socket in support of 3.3 V3V pins 2 and 4.  
10uP+0.1uP+0.01uP at the other end of the socket in support of 3.3 V3V pins 70 and 72.

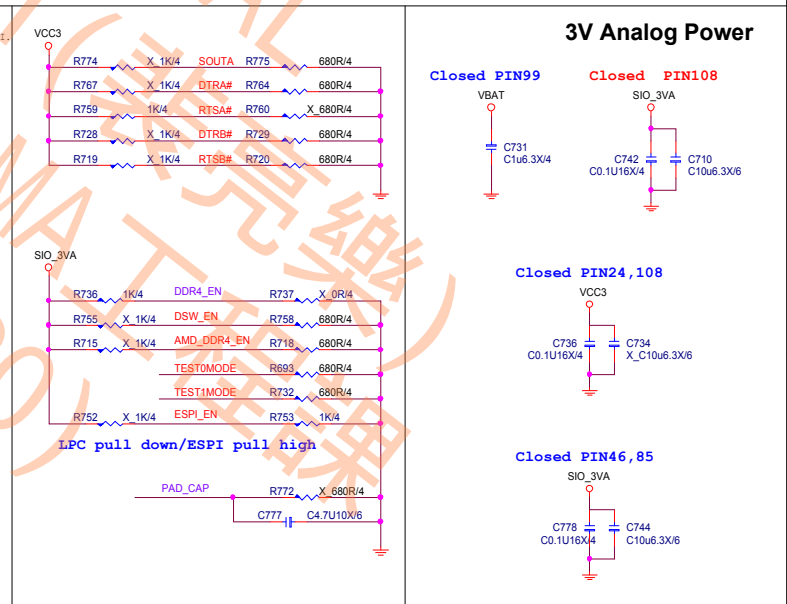
MICRO-STAR INT'L CO.,LTD			
MS-7B78			
Size	Document Description		Rev
Custom	M2_2 - WIFI+BT		10
Date: Tuesday, January 09, 2018		Sheet 28 of 77	





POWER ON STRAPPING PIN FOR NCT6797/6795					
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TESTMODE1_EN	ENABLE TESTMODE1_EN	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMD_DDR4_EN	AMD_DDR4_EN	DISABLE AMD DDR4 PWR	ENABLE AMD DDR4 PWR	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:  
If PIN34 strapping low, BIOS must programming LPT or GPIO

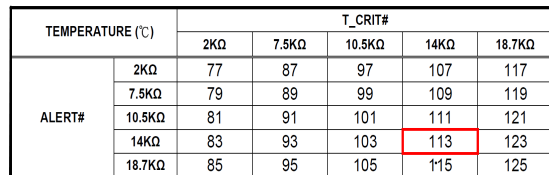


**MICRO-STAR INT'L CO.,LTD**

**MS-7B78**

Size Custom	Document Description	Rev 10
SIO - NCT6797D-M		
Date: Tuesday, January 06, 2016	Sheet 29	of 77

SIO HM Voltage over 2.048V will not detect


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/3.16K)) \\ &= 3.33V \end{aligned}$$

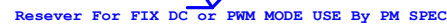

**MICRO-STAR INT'L CO.,LTD**

MS-7B78

Size Custom	Document Description <b>SIO - HW Monitor / NCT7718W</b>	Rev 10
Date: Tuesday, January 09, 2018		Sheet 30 of 77

**CPUFAN1**

- C3 Close to U2 PIN5  
If C3 place high thermal area, You can change X7R cap.

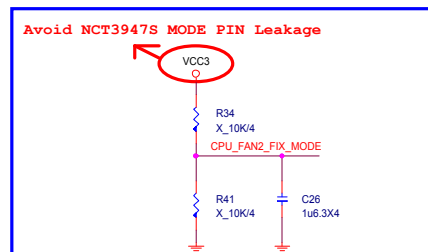


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

**PUMPFAN1**

1. PWM/DC/OCP LED
2. Mode GPIO BIOS can switch PWM/DC MODE
3. OCP connect GPIO for BIOS Use
4. FM:BIOS can read FAN PWM/DC MODE
5. CPUFAN1 LED OFF BLINK Use LED On/OFF



Resever For FIX DC or PWM MODE USE By PM SPEC

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

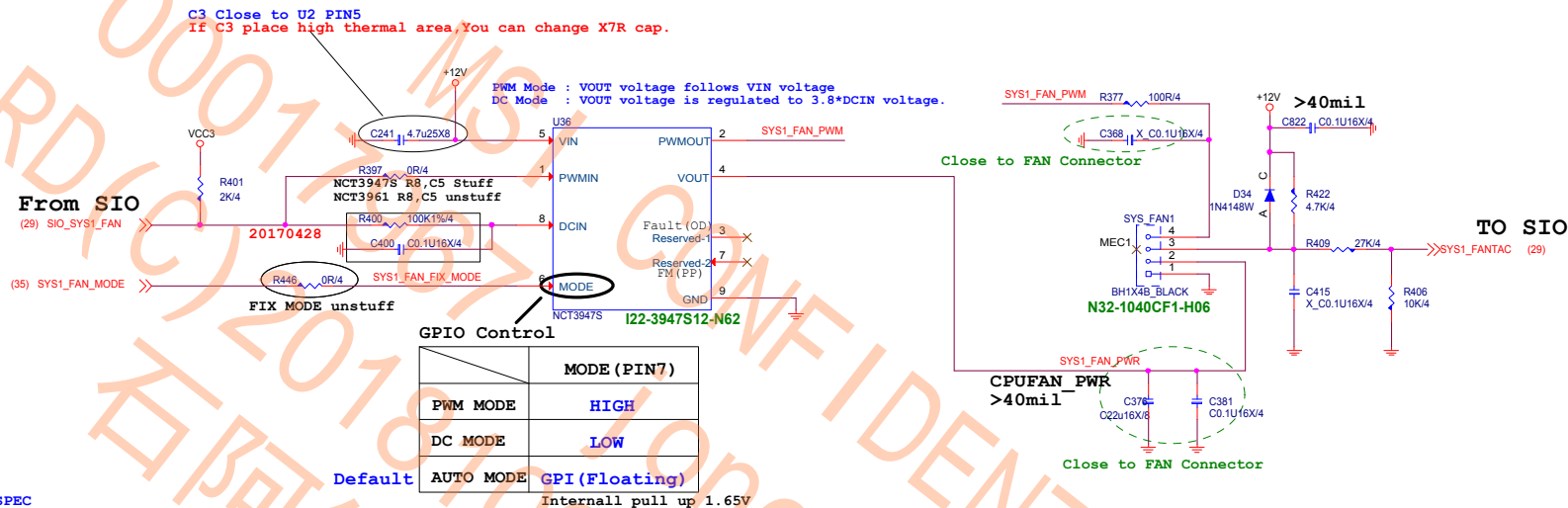
OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	
3.2~3.8A	10K	

CPUFAN2\_FAULT

# SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

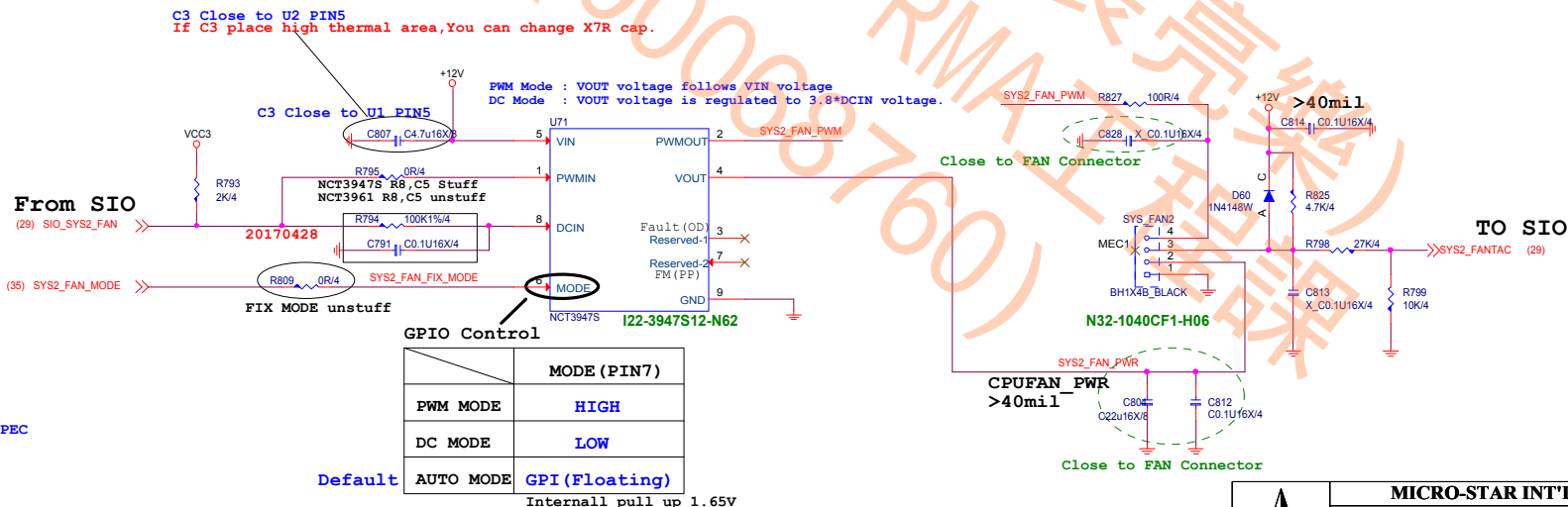
1.Mode GPIO BIOS can swtich PWM/DC MODE



# SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

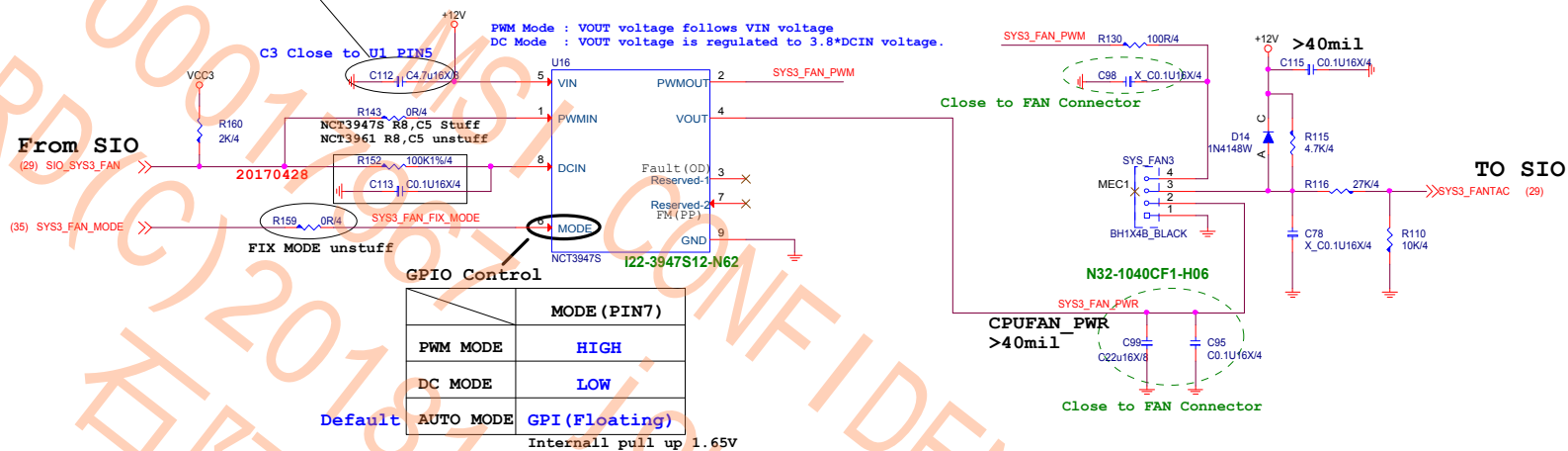
1.Mode GPIO BIOS can swtich PWM/DC MODE





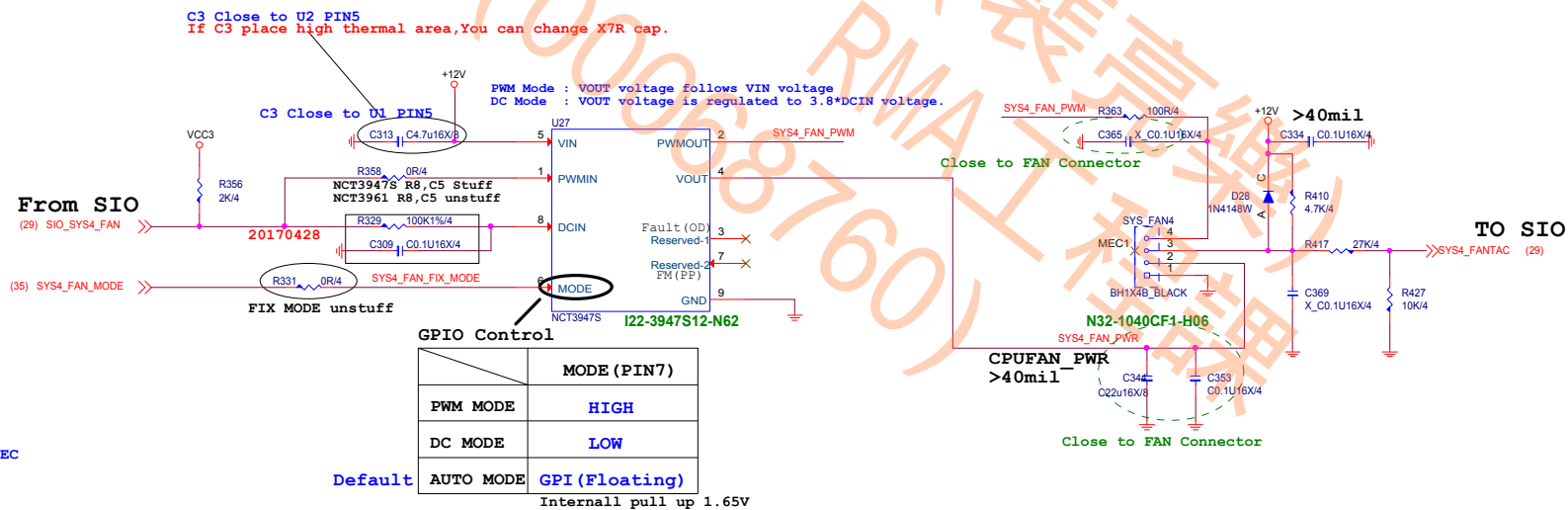
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

C3 Close to U2 PIN5  
If C3 place high thermal area, You can change X7R cap.



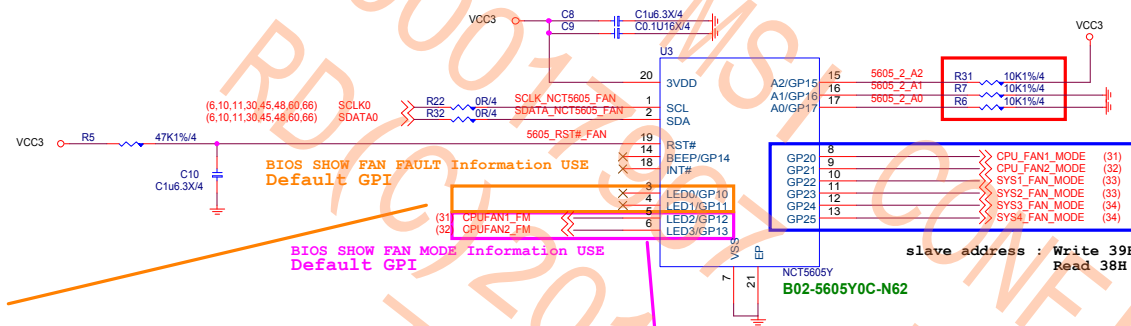
**TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE**

C3 Close to U2 PIN5  
If C3 place high thermal area, You can change X7R cap.



MS-7B78

Size Custom	Document Description <b>FAN TYPE-K SYSFAN3/4</b>	Rev 10
Date: Tuesday, January 09, 2018	Sheet 34 of 77	



By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

USE LED OFF & LED BLINK

Default GPI

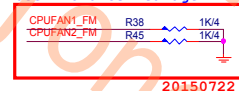
By PM Define FAN name

FAN MODE USE	FAN
GP20	CPUFAN1
GP21	CPUFAN2 PUMPFAN
GP22	SYSFAN1
GP23	SYSFAN2
GP24	SYSFAN3
GP25	SYSFAN4

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

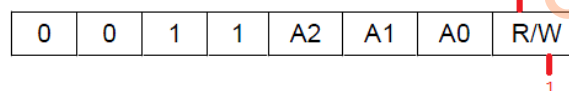
Use Avoid S5 leakage



## 1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power-on reset or from external reset.

NCT5605Y SMBus™ Address is:

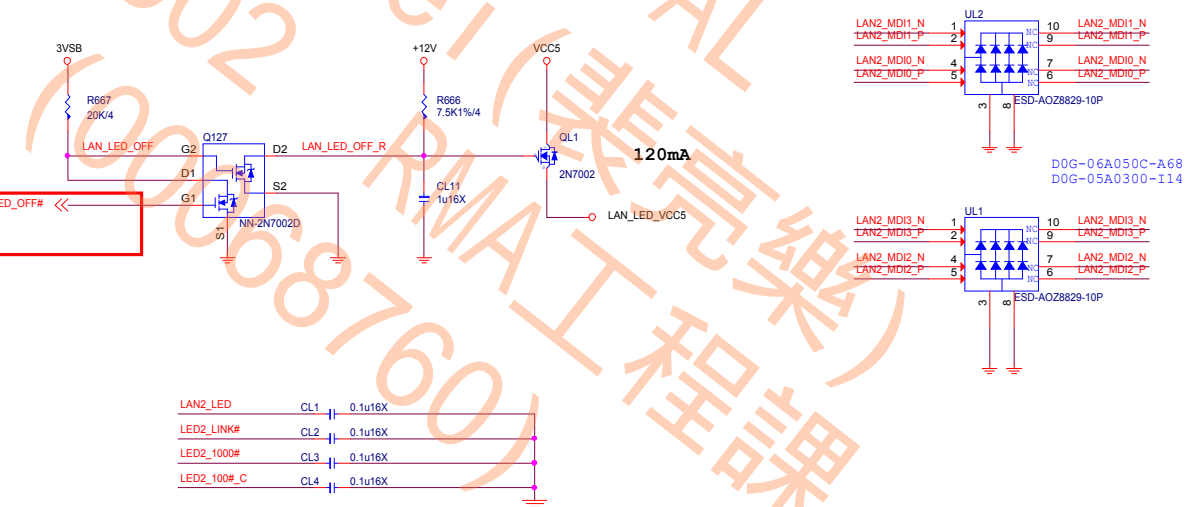
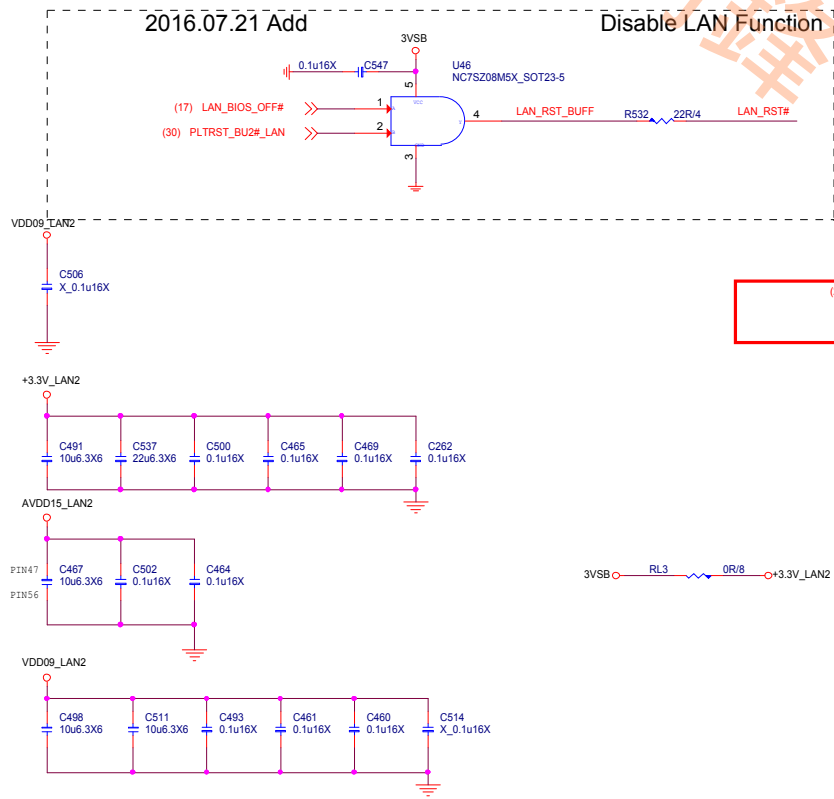
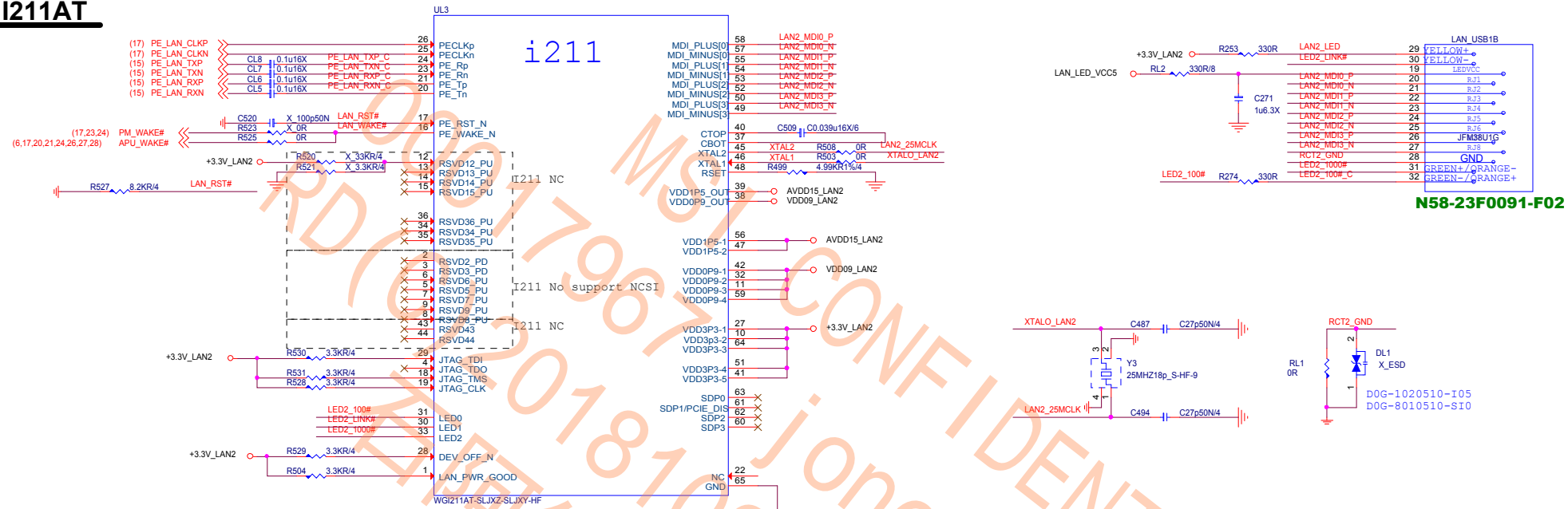


MICRO-STAR INT'L CO.,LTD

MS-7B78

Size Custom	Document Description	Rev 10
Date: Tuesday, January 09, 2018	FAN GPIO NCT5605	Sheet 35 of 77

**LAN-- I211AT**



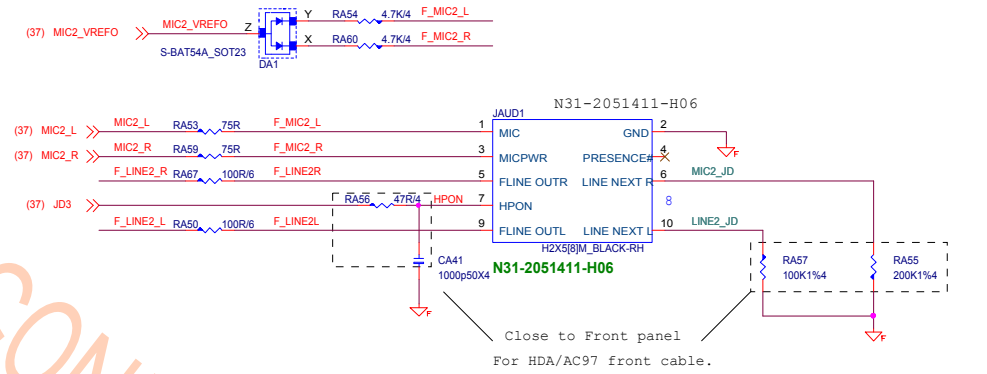
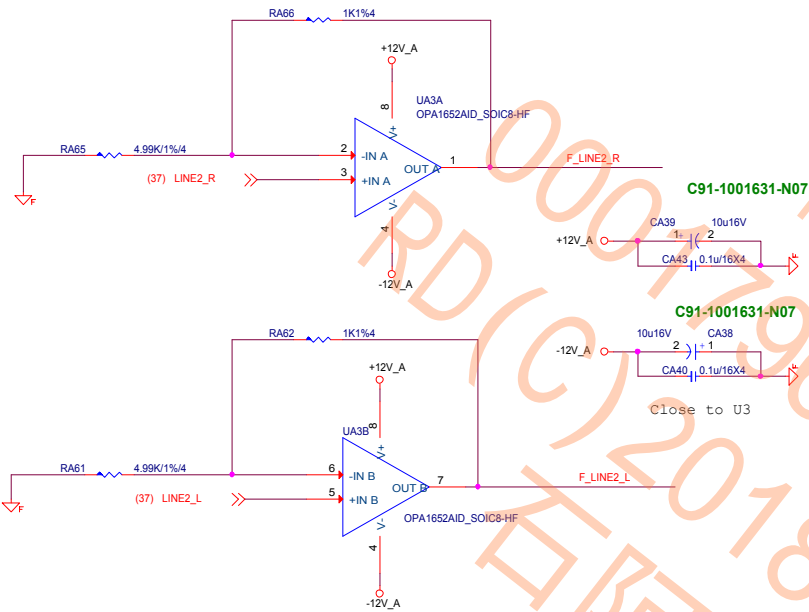
**MICRO-STAR INT'L CO.,LTD**

MS-7B78

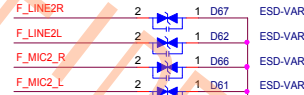
Size	Document Description	Rev
Custom	<b>LAN - I211AT</b>	10

Date: Tuesday, January 09, 2018	Sheet 36 of 77
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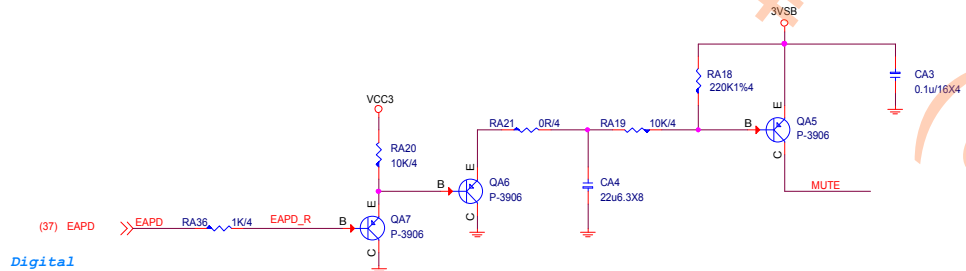


Close to Jack  
ESD protect

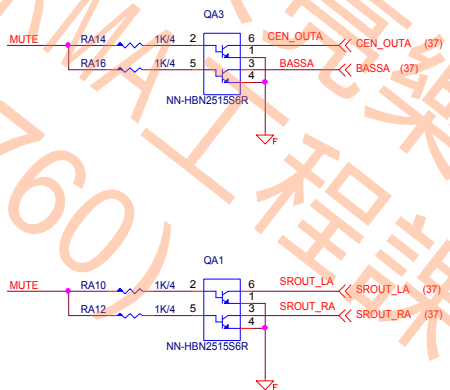


#### Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)



(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change SROUT\_LA, SROUT\_RA, CEN\_OUTA, BASSA to TVS)



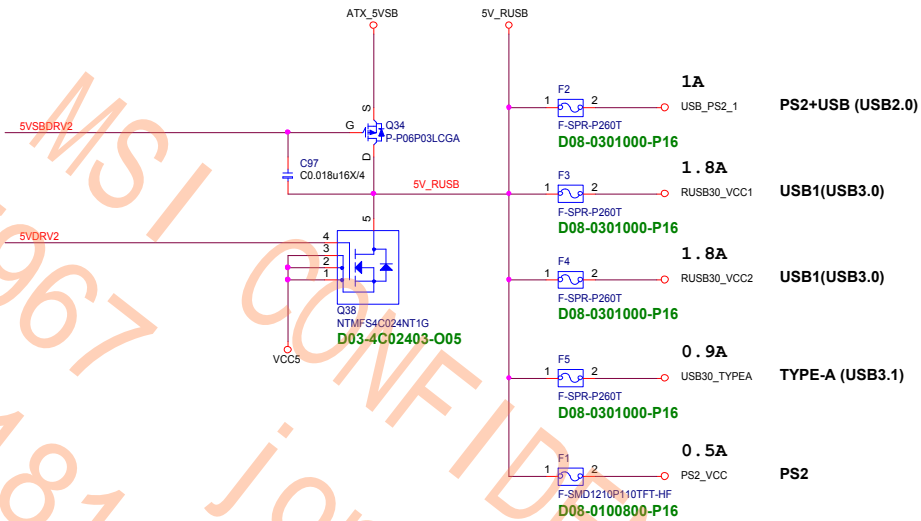
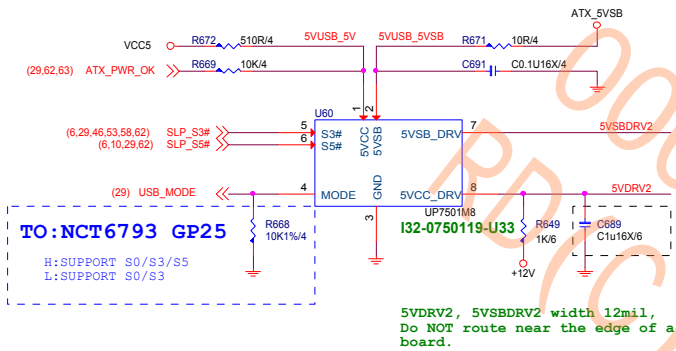
Audio moat is transparent and width 40mil



MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size	Document Description	Rev
Custom	Audio DePop	10
Date: Tuesday, January 09, 2018	Sheet 38 of 77	

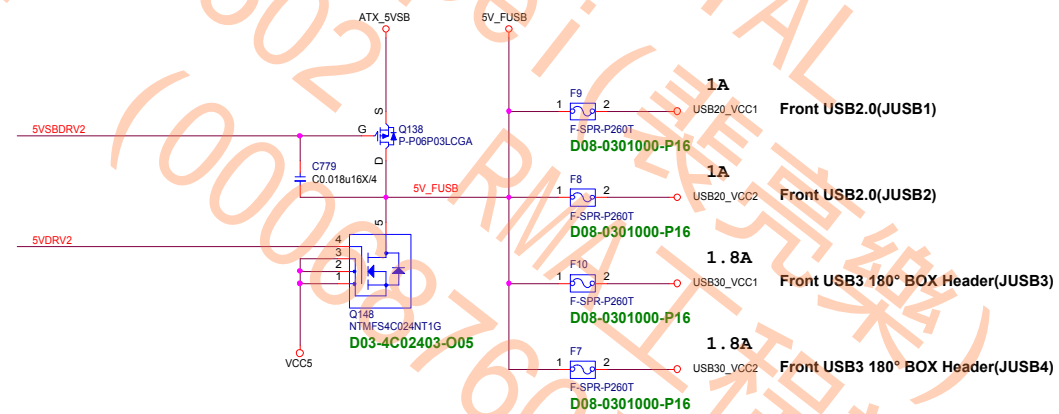


## USB Power



### Rear (5.1A)

### Front (5.6A)



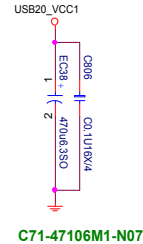
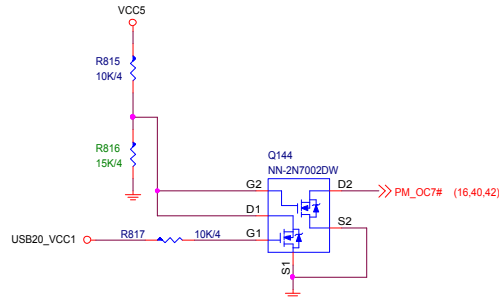
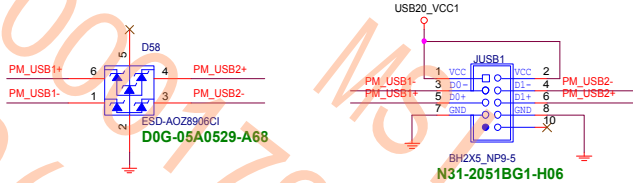
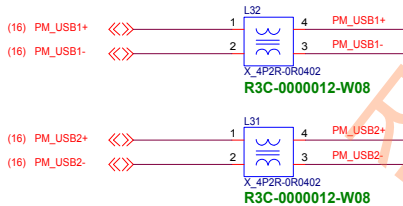
**MICRO-STAR INT'L CO.,LTD**

MS-7B78

Size Custom	Document Description <b>USB Power - UP7501</b>	Rev 10
Date: Tuesday, January 09, 2018		Sheet 39 of 77

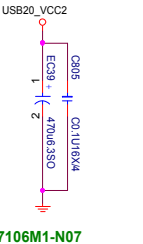
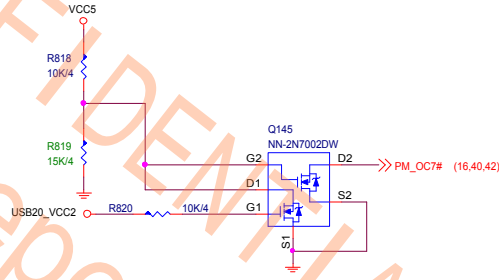
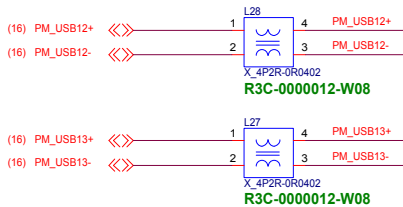
Front USB2.0 (JUSB1)

5V@1A



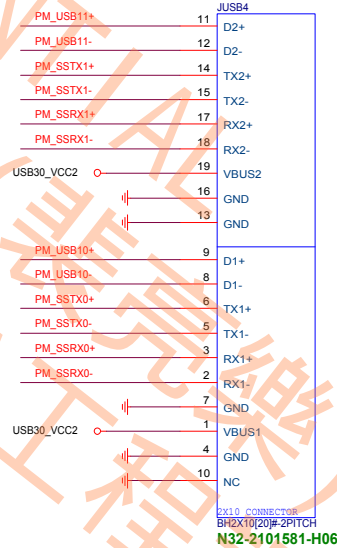
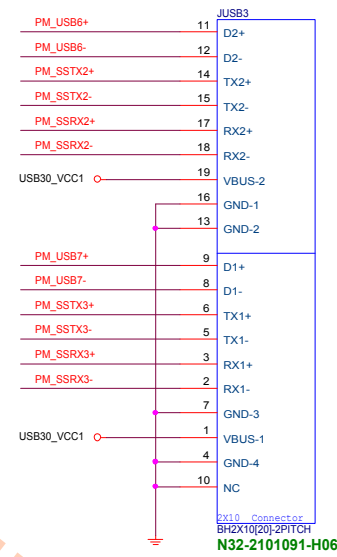
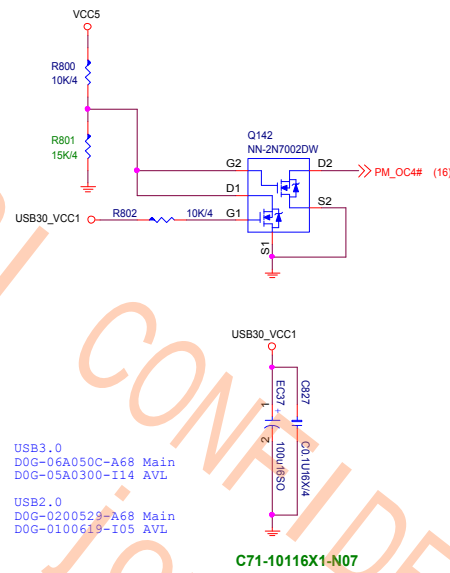
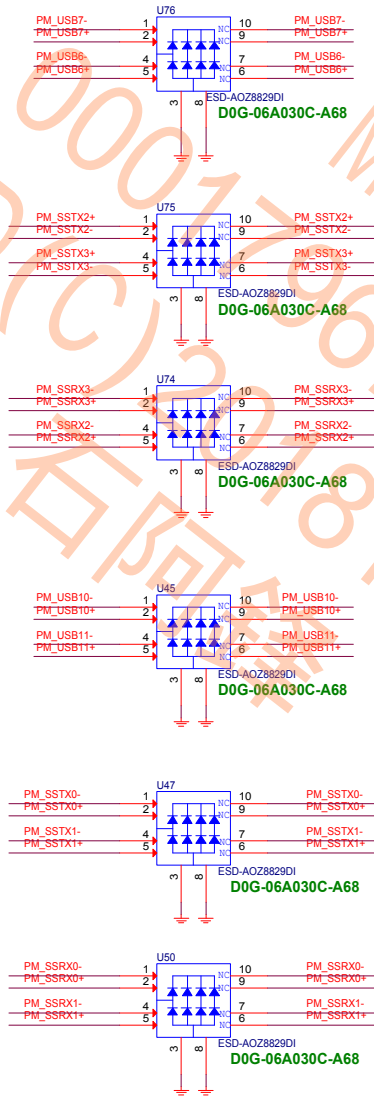
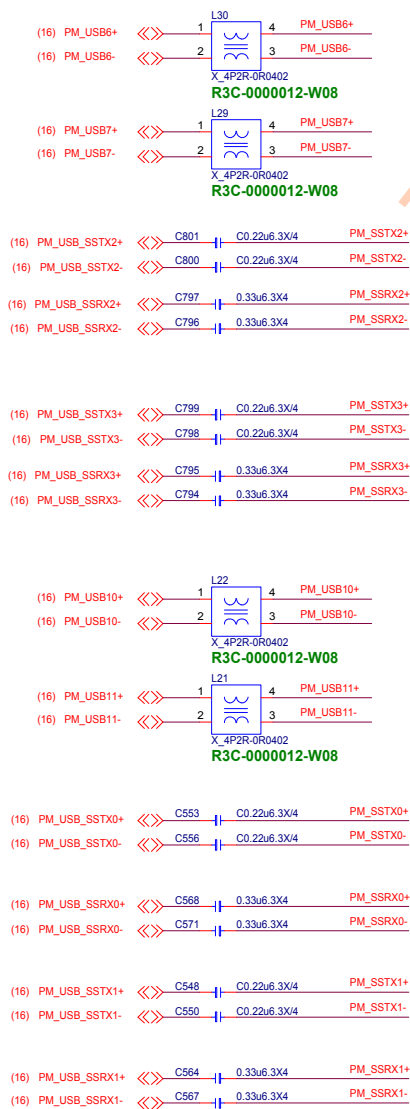
Front USB2.0 (JUSB2)

5V@1A



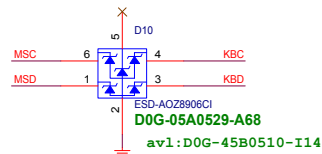
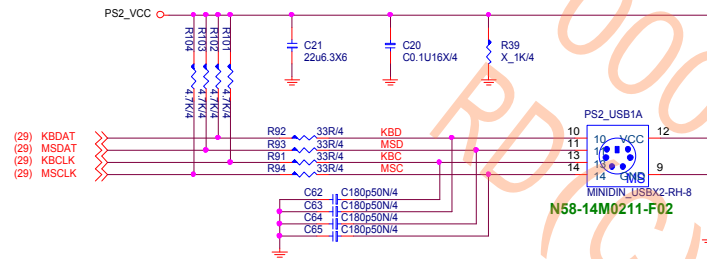
# Front USB3 180° BOX Header(JUSB3)

5V@1.8A

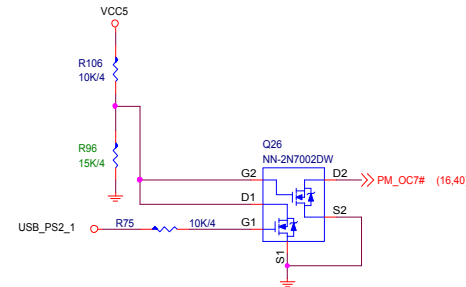
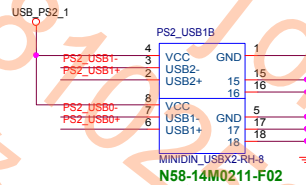
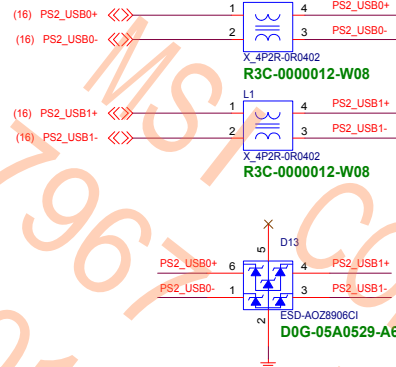


# PS2+USB (USB2.0)

5V@1A



layout note:  
C21 must close to TVS pin5  
TVS must near KB MS1 connector and route without branch  
Varistor must close to TVS and route without branch

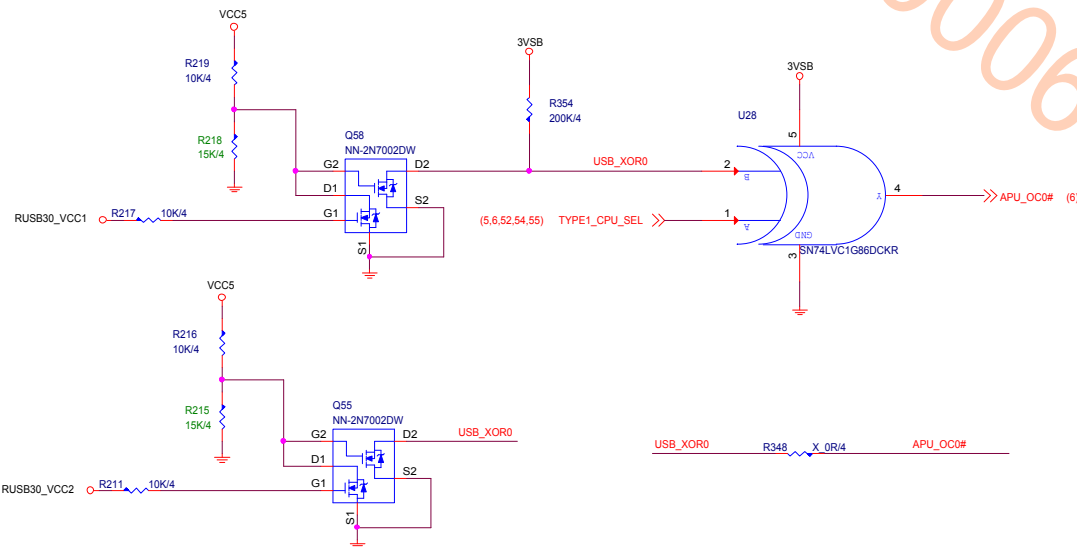
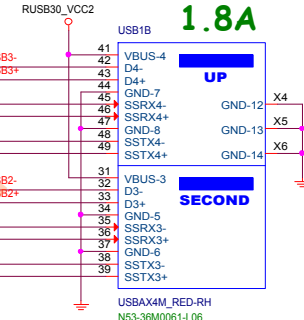
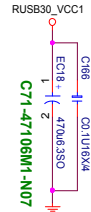
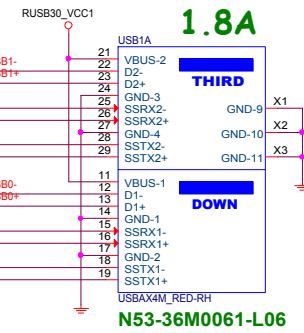
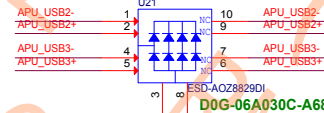
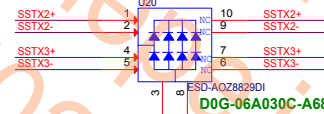
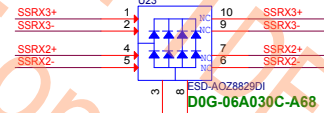
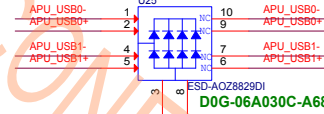
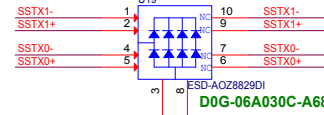
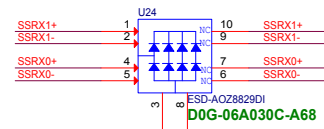
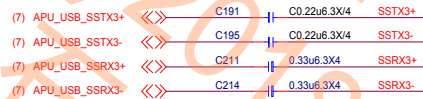
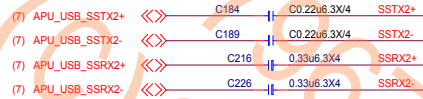
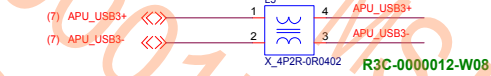
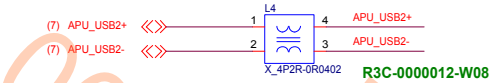
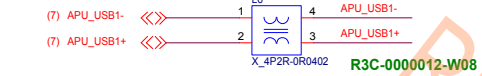
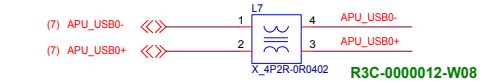


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MS-7B78

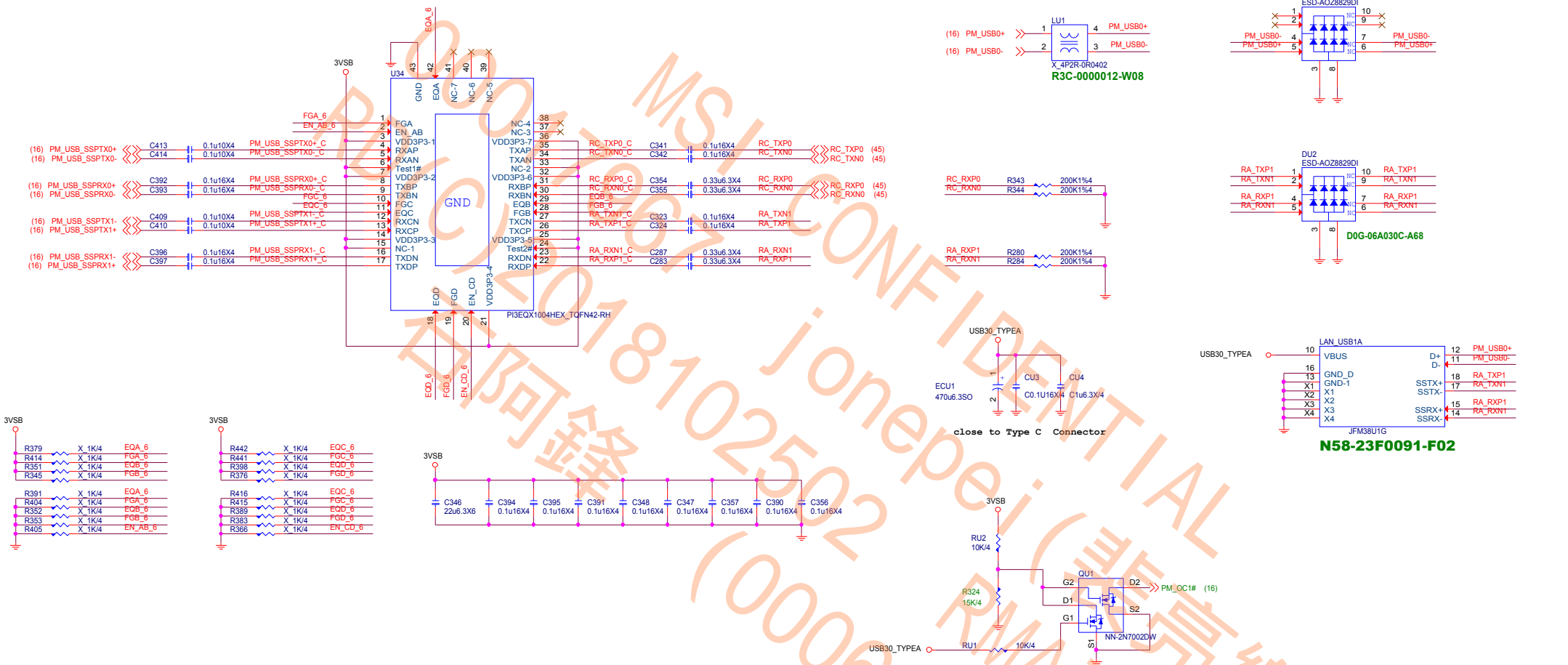
Size	Document Description	Rev
Custom	Rear USB2.0 + PS2	10
Date:	Tuesday, January 09, 2018	Sheet 42 of 77

# Rear USB3.0 GEN1 5V@1.8A



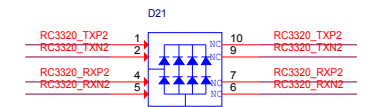
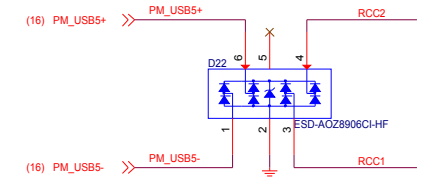
	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

# TYPE-A PI3EQX1004 Redriver



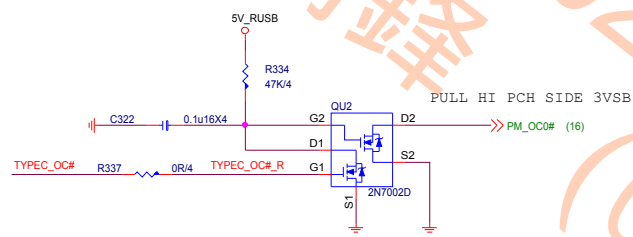
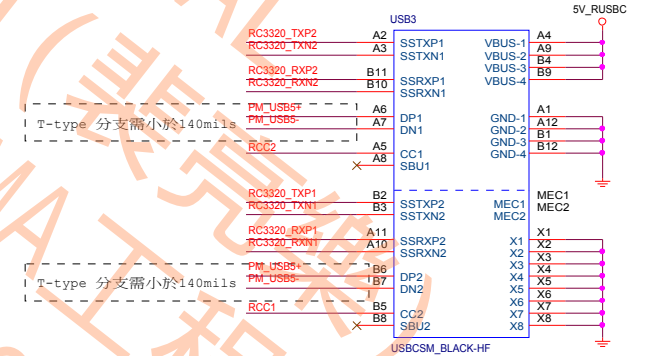
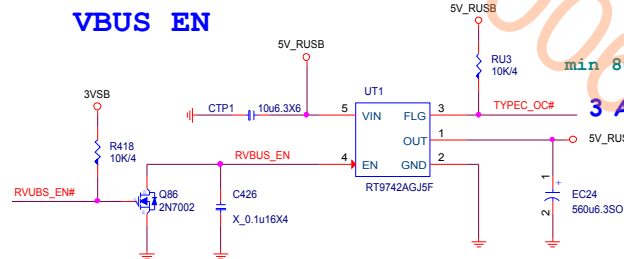
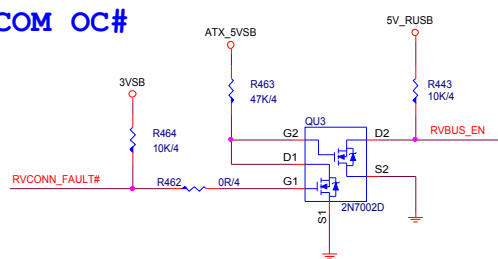


## USB Type-C MUX with Configuration Channel (CC)



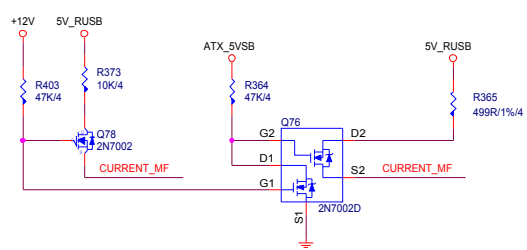
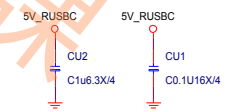
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D0G-05A0300-II4 AVL  
D0G-45B031C-005 AVL

5V\_USB  
R334  
47KΩ  
OU2  
PULL HI PCH SIDE 3VSB

[illegible]

**N53-24M0040-L06**

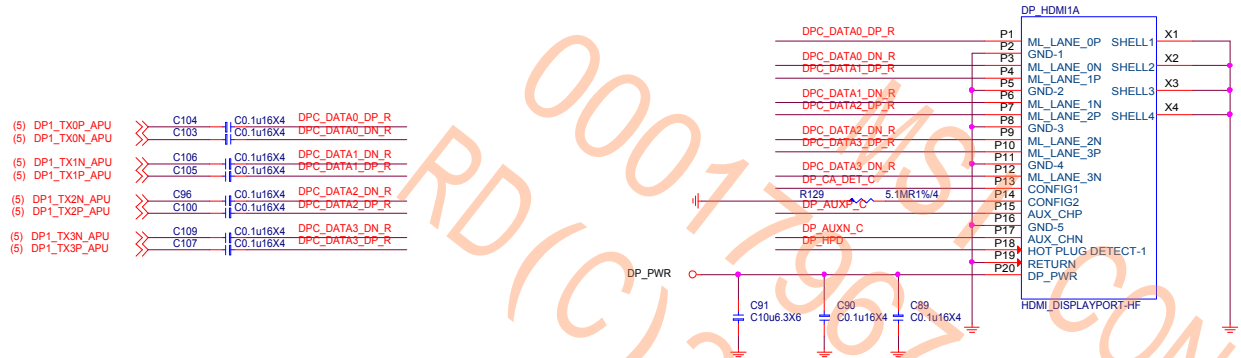
close to Type C Connector



MS-7B78

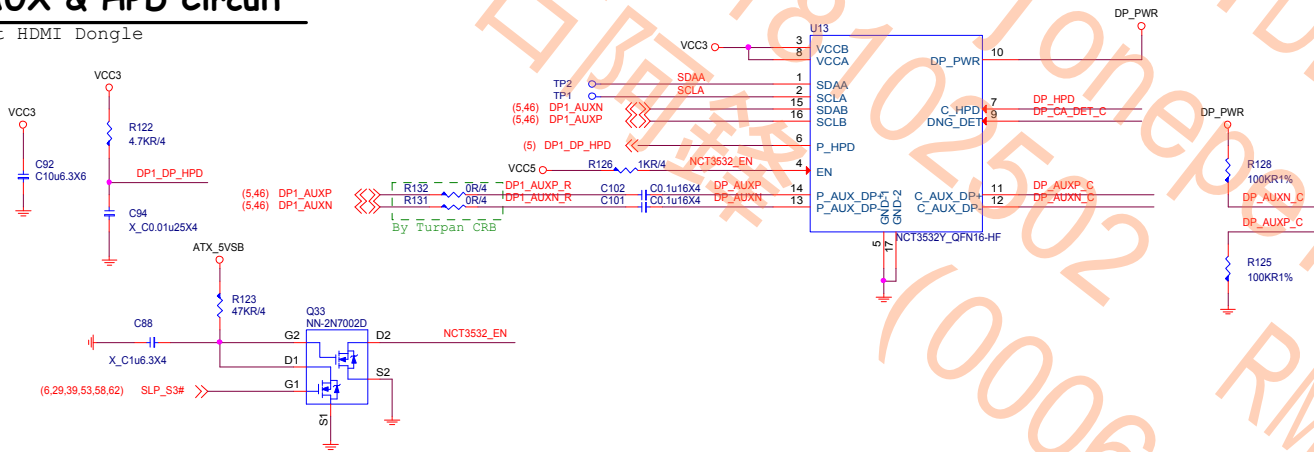
Size Custom	Document Description <b>Rear USB3.1 Type C / mux</b>	Rev 10
Date: Tuesday, January 09, 2018		Sheet 45 of 77

DP CONNECTOR

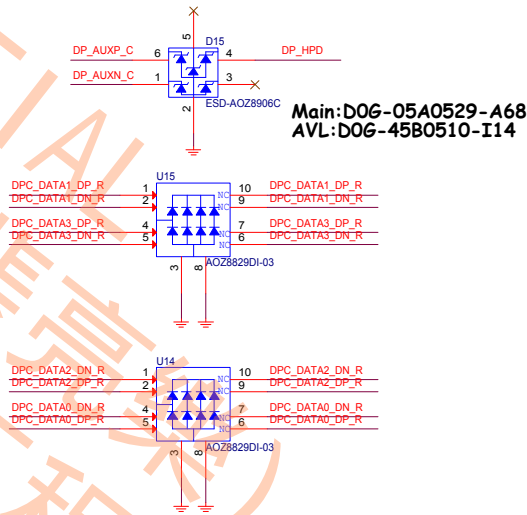


DP AUX & HPD Circuit

Support HDMI Dongle



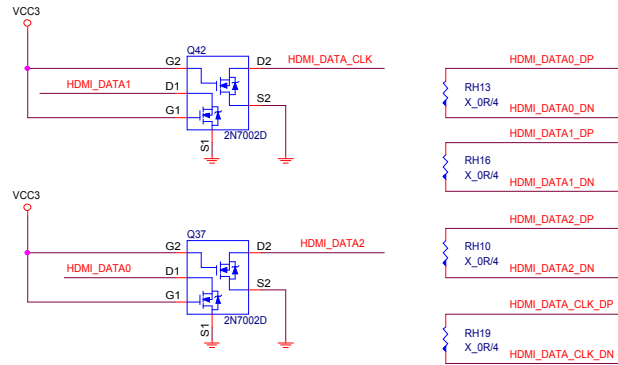
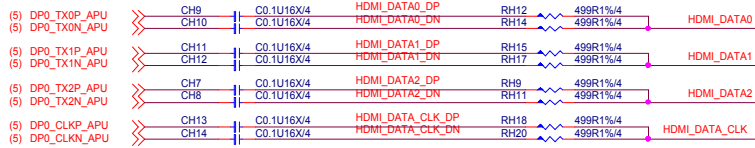
ESD



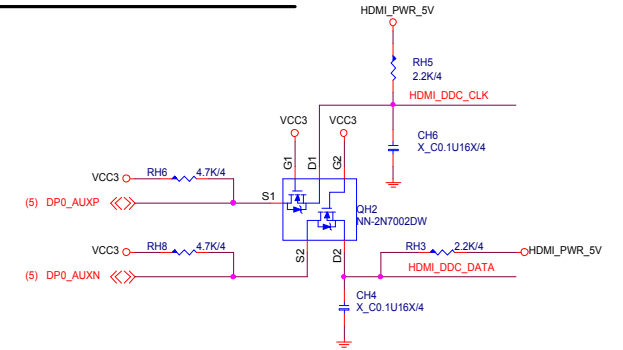
MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size	Document Description	Rev
Custom	DP	10
Date:	Tuesday, January 09, 2018	Sheet 46 of 77

# HDMI CONNECTOR

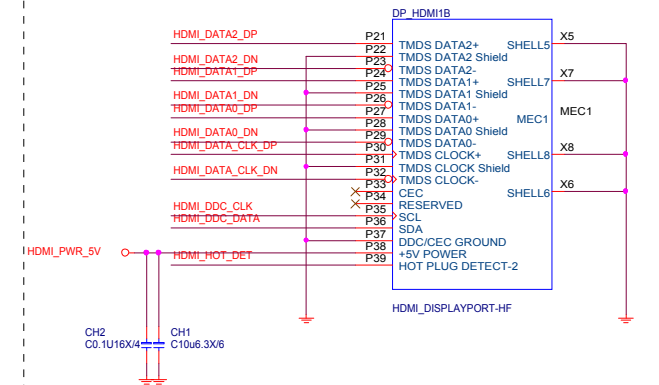
For HDMI 1.4



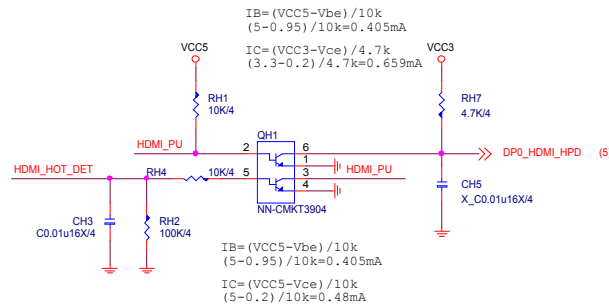
## AUX Level Shifter



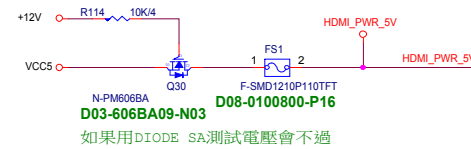
## Connector



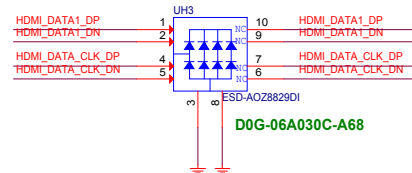
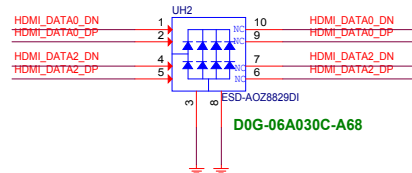
## HPD Circuit



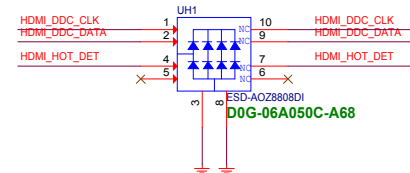
## Connector Power

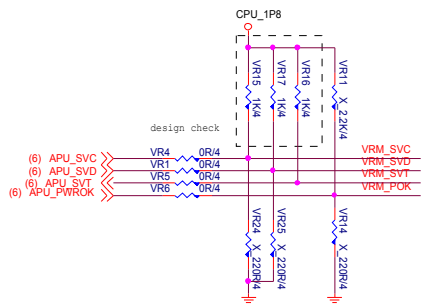


## For EMI



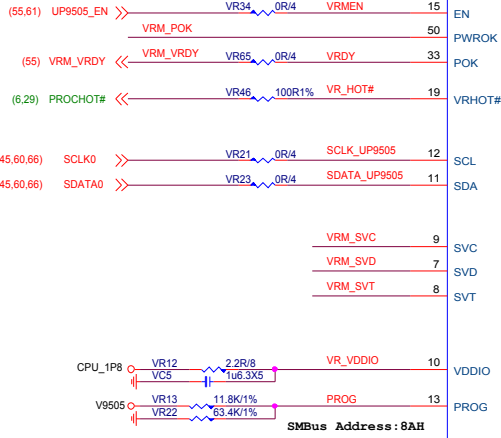
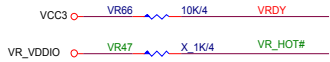
## 注意:耐壓5v零件



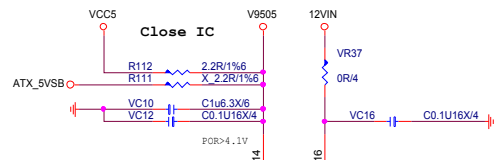
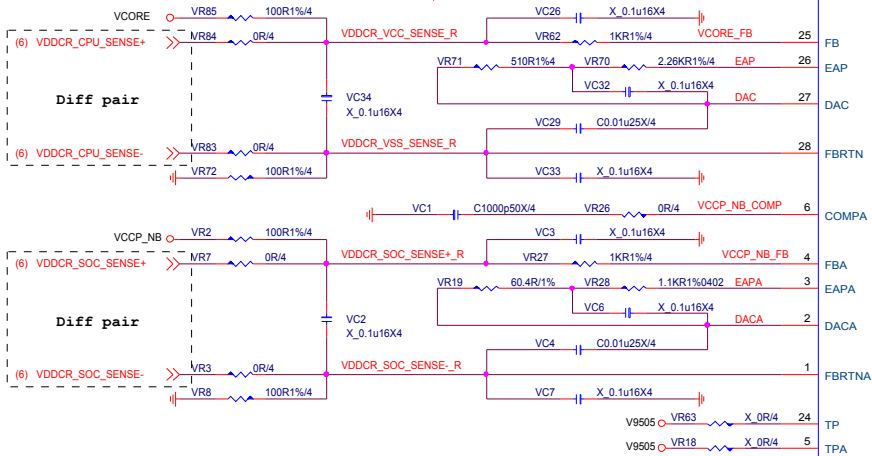


Note:VID Override Circuit

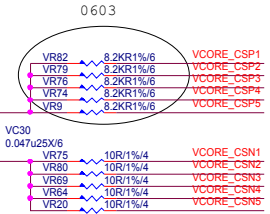
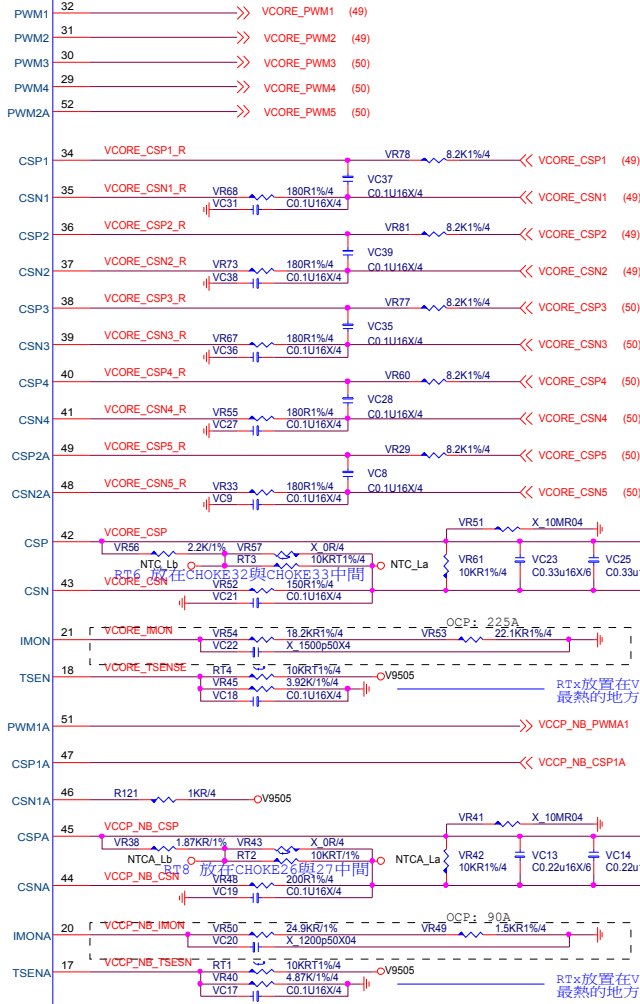
BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



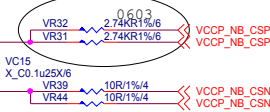
Switching Frequency = 300KHz



Vcore: ICCMax 140A  
LL: 0.78mohm  
OCP: 225A  
  
SOC: ICCMax 75A  
LL: 1.26ohm  
OCP: 90A

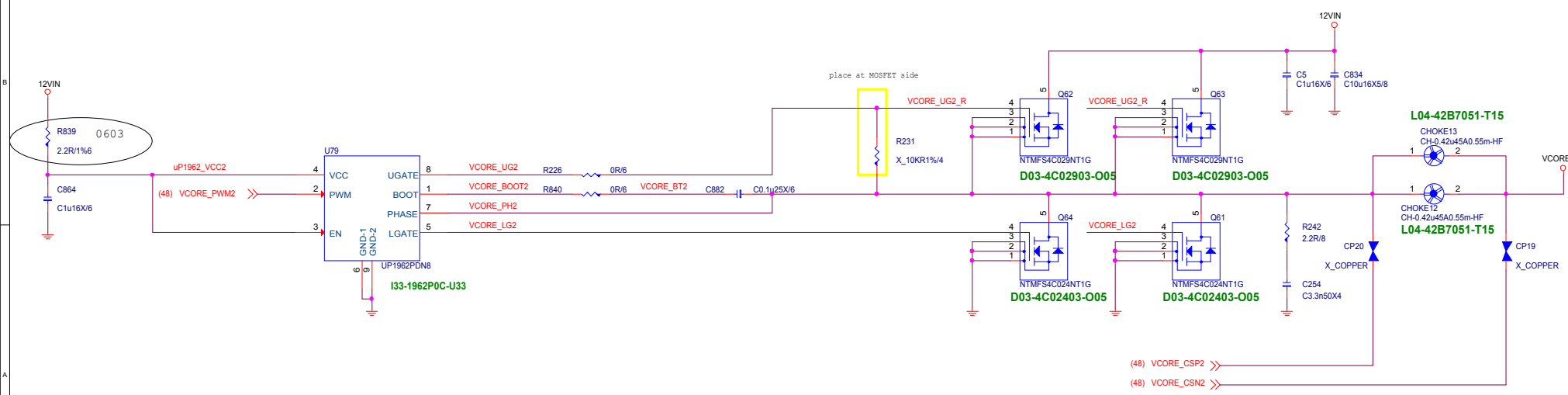
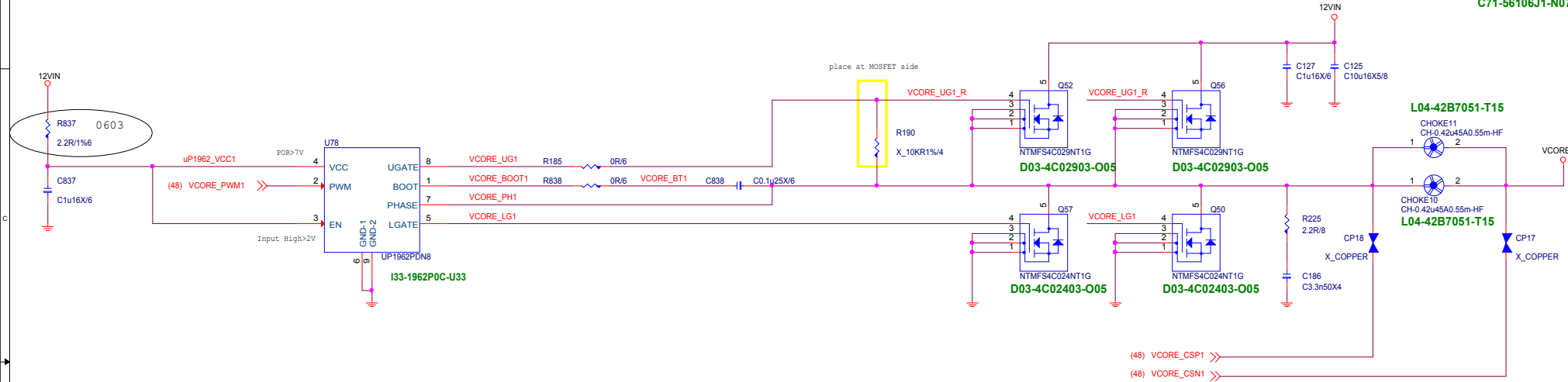
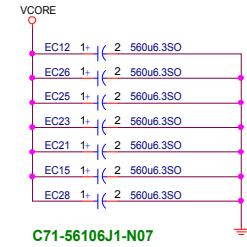


Vcore則是125度觸發，115度恢復



NB項MOS最高溫會在115度VRHOT拉low，並在90度恢復

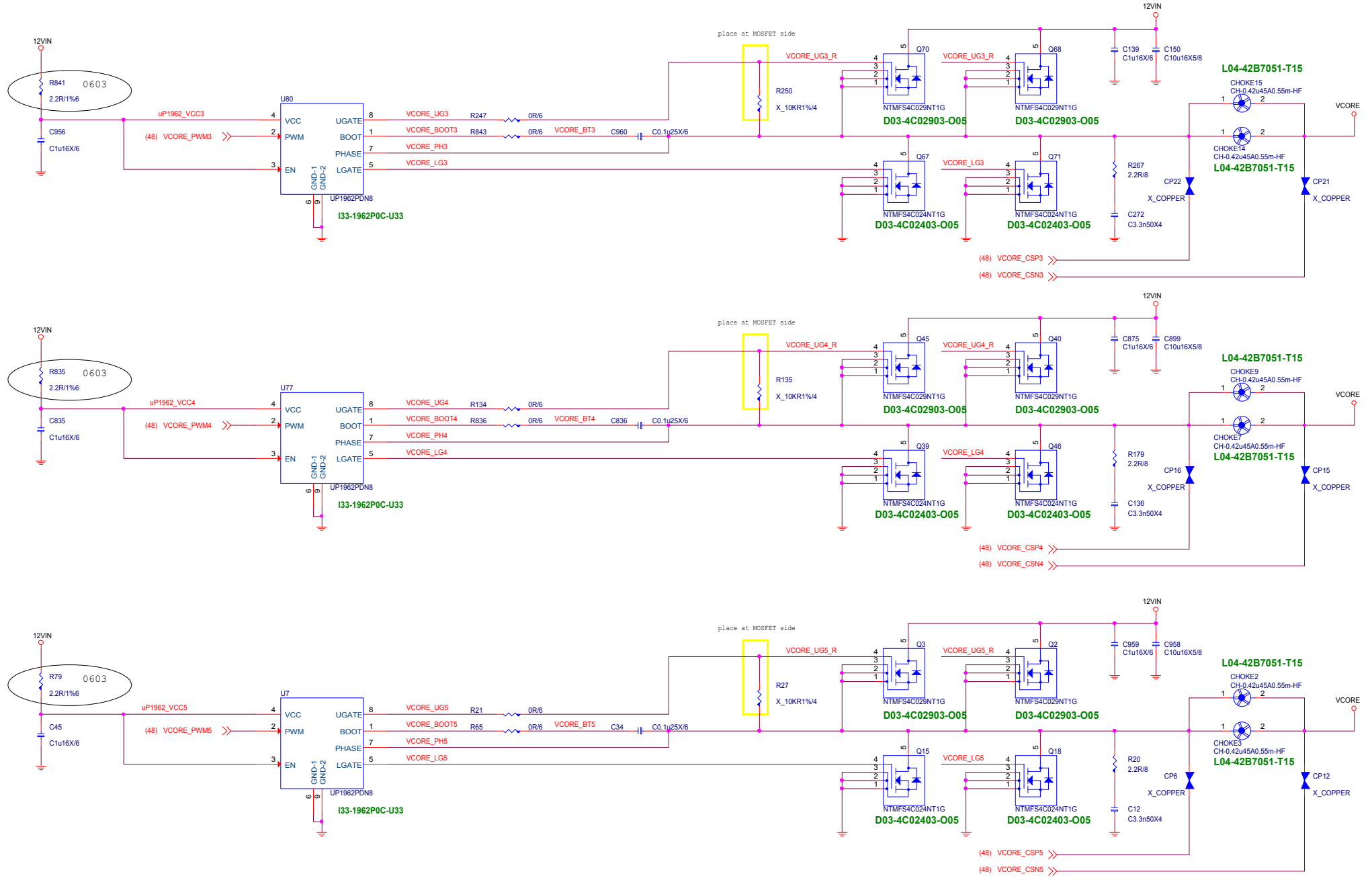
VCORE 105W TDC:95A EDC:140A



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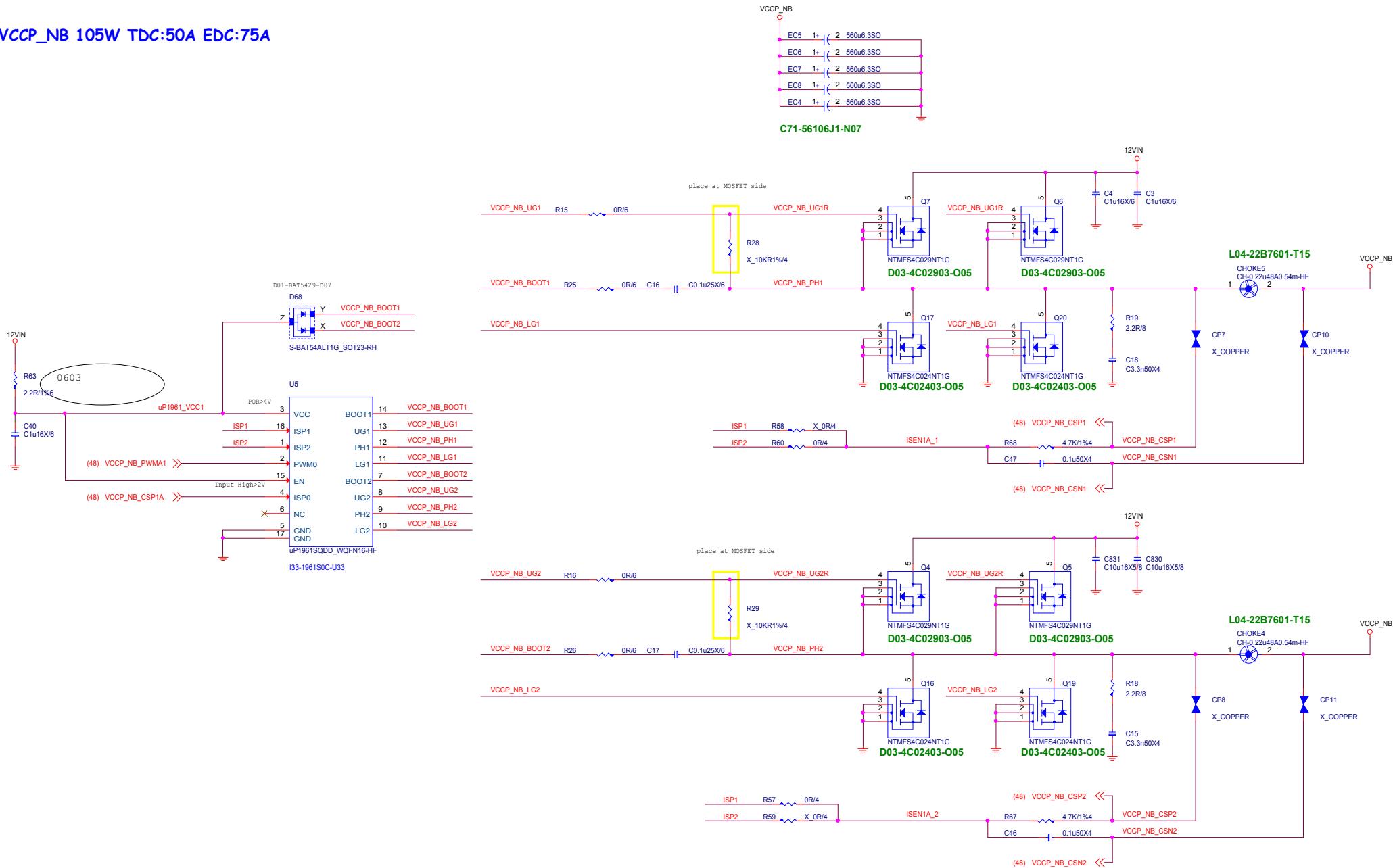
MS-7B78

Size	Document Description	Rev
Custom	CPU Power Phase 1 - 4	10
Date: Tuesday, January 09, 2018	Sheet 49 of 77	





# VCCP\_NB 105W TDC:50A EDC:75A



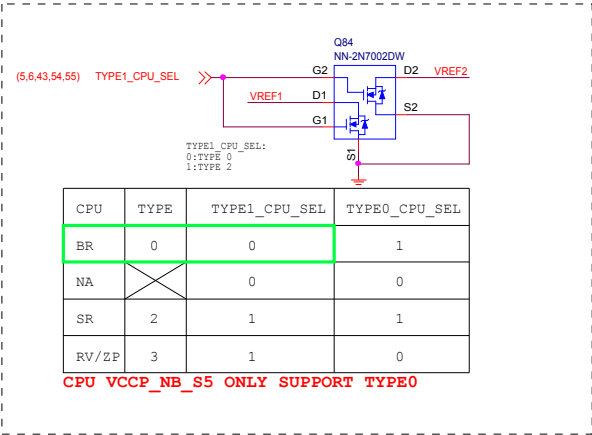
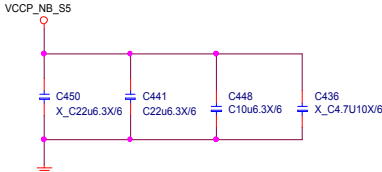
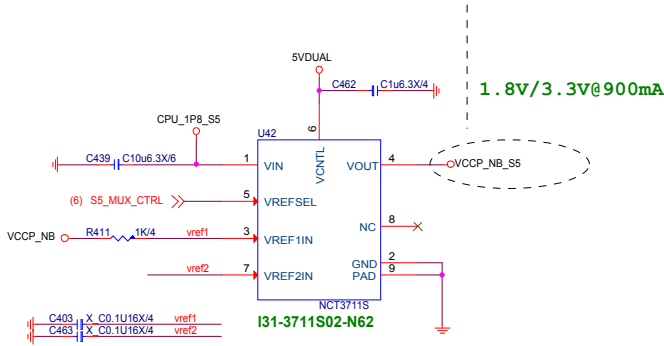
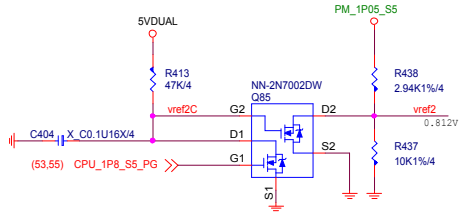
MICRO-STAR INT'L CO.,LTD			
MS-7B78			
Size	Document Description		Rev
Custom	CPU Power NB 1 - 2		10
Date:	Tuesday, January 09, 2018	Sheet	51 of 77

FOR  
VCCP\_SOC\_S5

S5\_MUX\_CTRL  
HIGH:S0  
LOW: S3/S5

H: +VDDCR\_FCH ALW will track VDDNB  
L: If VDDCR\_SOC<0.775V (OR 0.85V),VDDCR\_SOC\_S5 =0.775V.  
If VDDCR\_SOC >= 0.775V (OR 0.85V) , VDDCR\_SOC\_S5 will track VDDCR\_NB

(VDDCR\_SOC\_S5 is only used for AMD Family 15h Models 60h-6Fh processors)

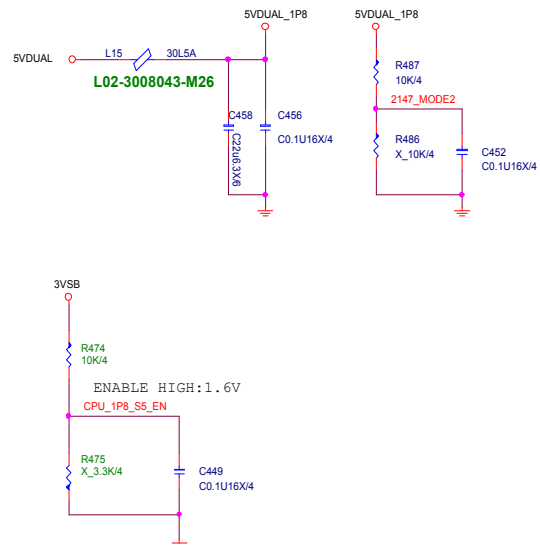


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

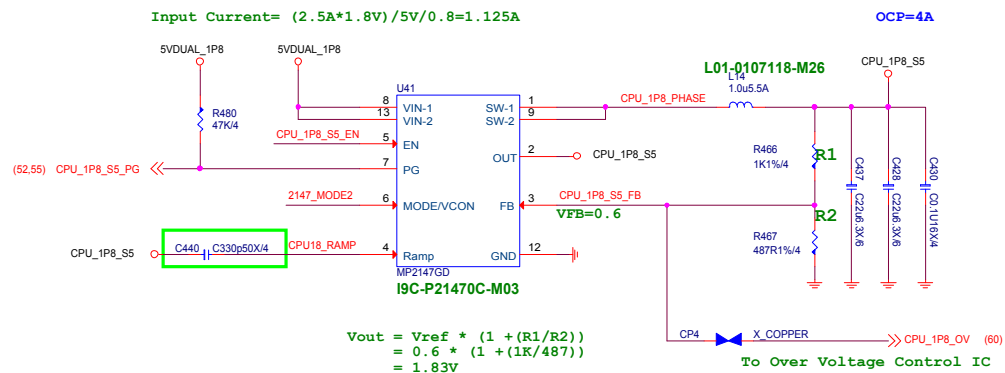
CPU VCCP\_NB\_S5 ONLY SUPPORT TYPE0



1.8V S5@0.5A

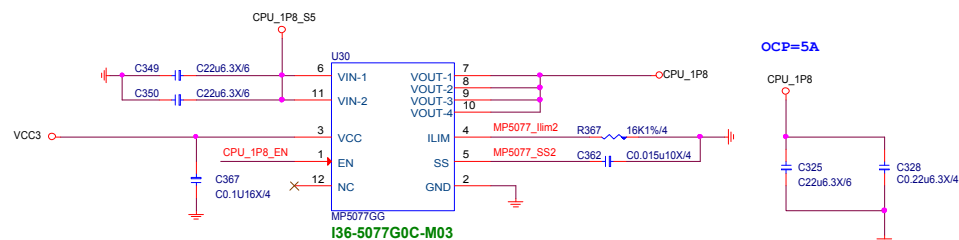
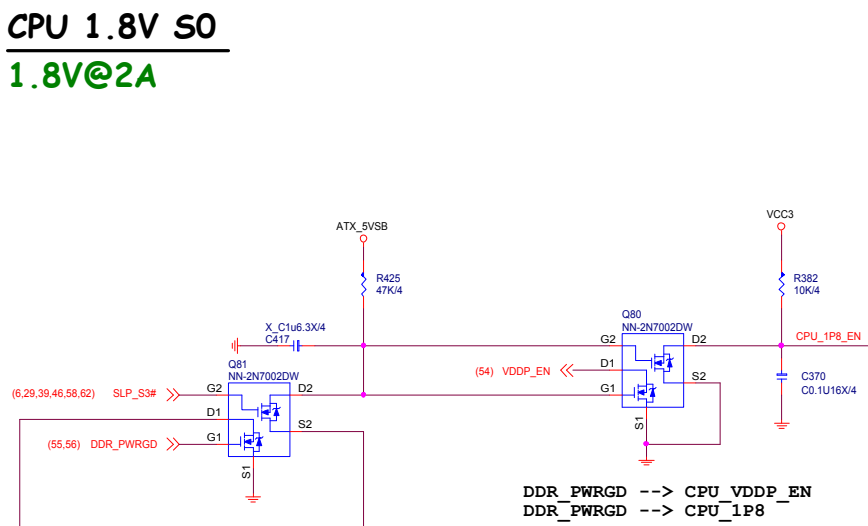


Input Current=  $(2.5A \cdot 1.8V) / 5V / 0.8 = 1.125A$



$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (1K/487)) \\ &= 1.83V \end{aligned}$$

1.8V@2A



$$I_{limit} = (1/R_{limit}) * S, S = 80000, \text{when } V_{IN} = 1.05V$$
$$= (1/16) * 80000 = 5.0375A$$

$$T_{ss} = (1/3) * ((V_{out} * C_{ss}) / I_{ss}), I_{ss} = 9\mu A$$

$$T_{ss} = (1/3) * ((1.8 * 15n) / 9\mu A) = 1ms$$



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MS-7B78

Size	Document Description	Rev
Custom	CPU Power 1.8_S0/S5	10
Date: Tuesday, January 09, 2018		Sheet 53 of 77

# CPU\_VDDP\_S0

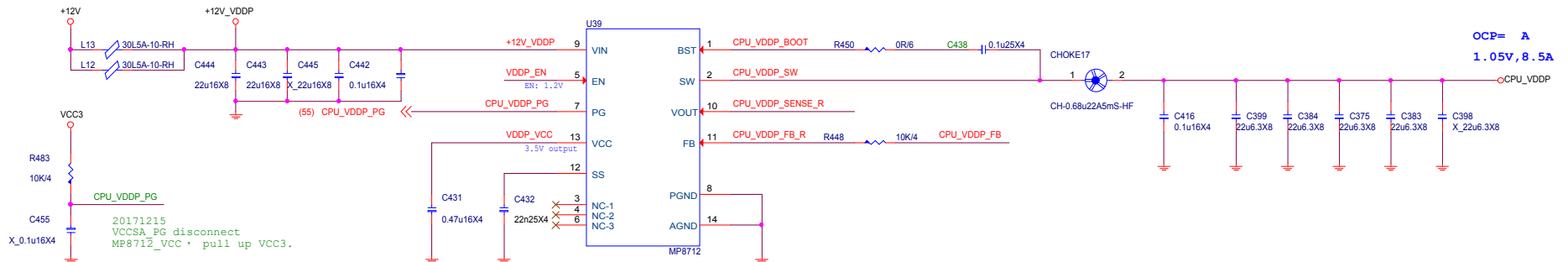
1.05V/0.9V@S0:8.5A

S0:8.5A  
S5:1A

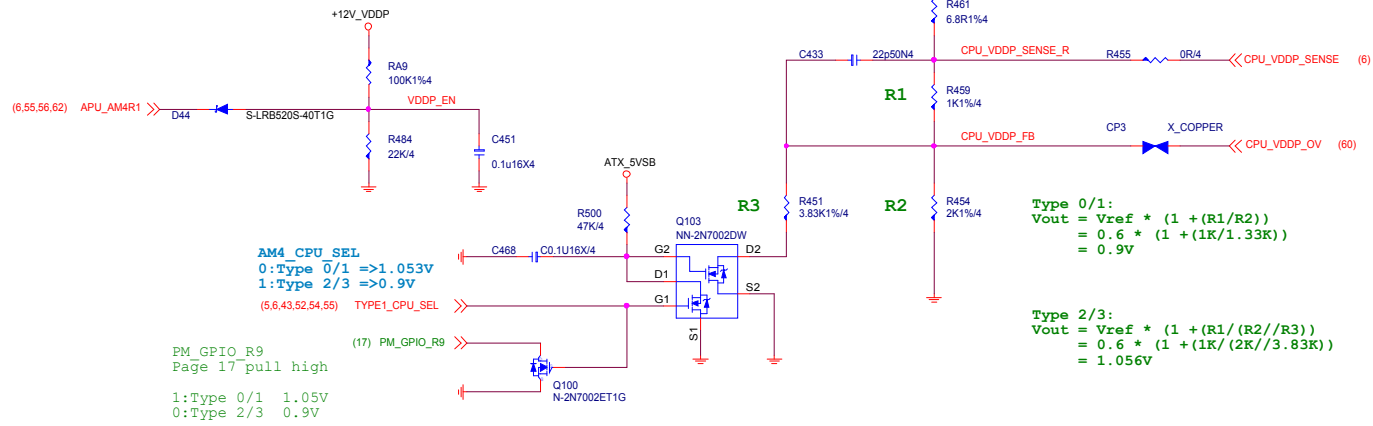
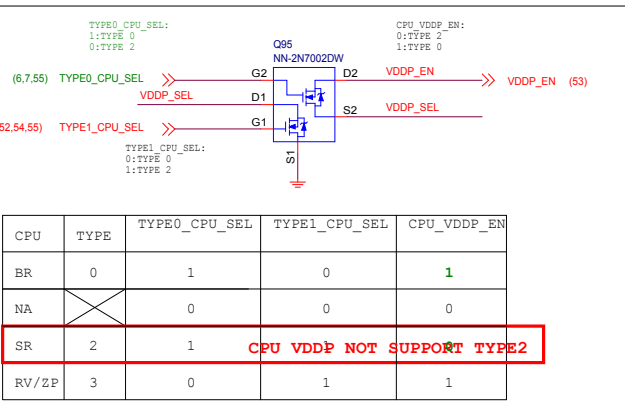
OCP=14A

$I_{in} = 11.1A * 1.05V / 0.8 / 12V = 1.21A$   
L02-3008043-M26  
Over 85°C , Rated Current  
1.5A.

Input Current= (8.5A\*1.05V)/12V/0.8=2.23A



OCP= A  
1.05V, 8.5A



Type 0/1:  
 $V_{out} = V_{ref} * (1 + (R1/R2))$   
 $= 0.6 * (1 + (1K/(1.33K)))$   
 $= 0.9V$

Type 2/3:  
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$   
 $= 0.6 * (1 + (1K/(2K//3.83K)))$   
 $= 1.056V$

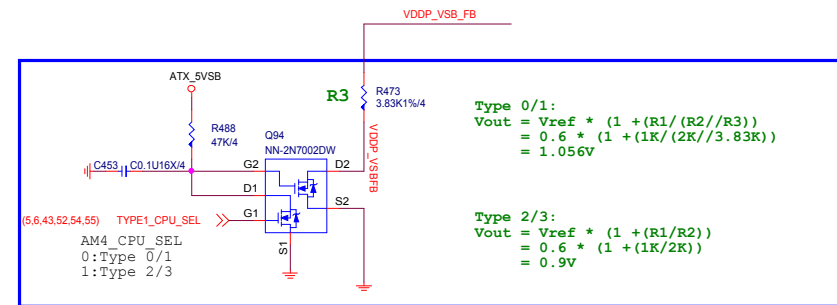
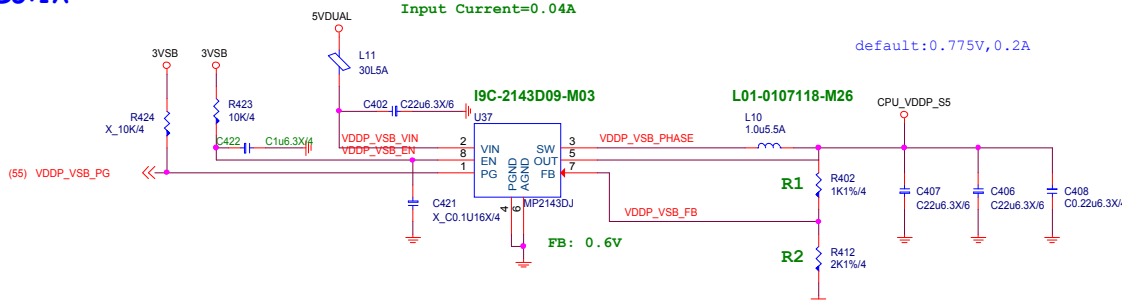
# CPU\_VDDP\_S5

(VDDCR\_SOC\_S5)

1.05V/0.9V  
S5:1A

Input Current=0.04A

default:0.775V,0.2A



Type 0/1:  
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$   
 $= 0.6 * (1 + (1K/(2K//3.83K)))$   
 $= 1.056V$

Type 2/3:  
 $V_{out} = V_{ref} * (1 + (R1/R2))$   
 $= 0.6 * (1 + (1K/(2K)))$   
 $= 0.9V$



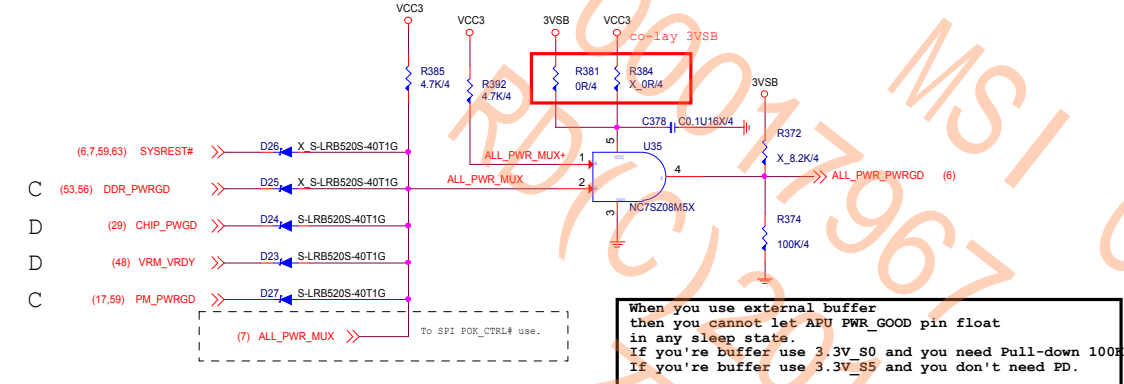
MICRO-STAR INT'L CO.,LTD

MS-7B78

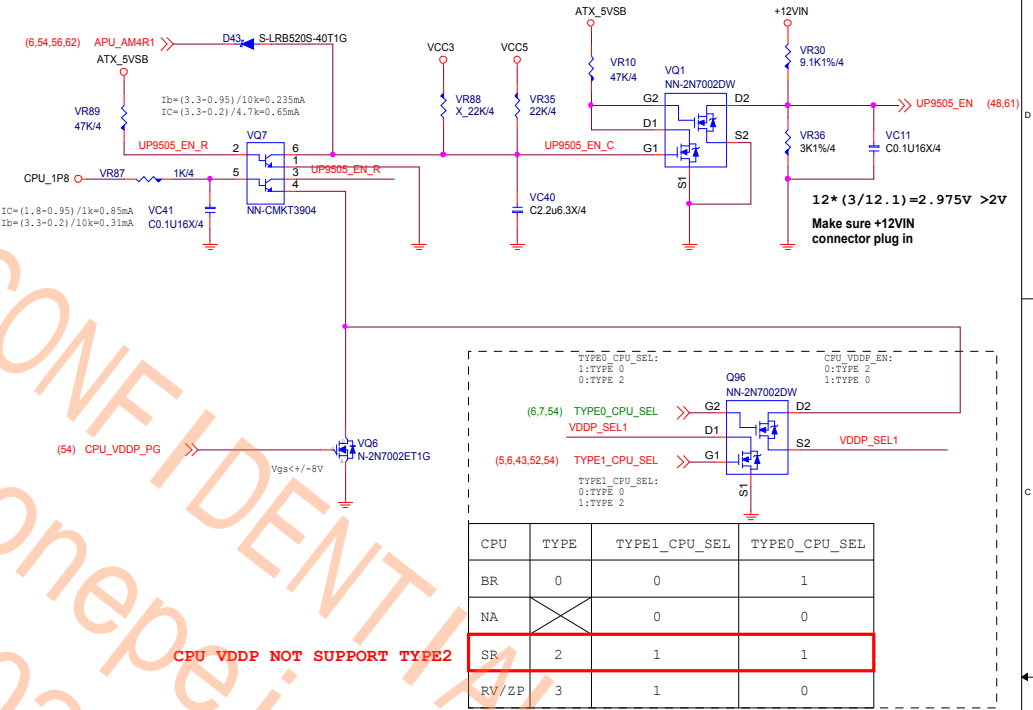
Size	Document Description	Rev
Custom	CPU Power VDDP - TPSS6C215	10
Date:	Tuesday, January 08, 2018	Sheet 54 of 77

ALL POWER GOOD MUX

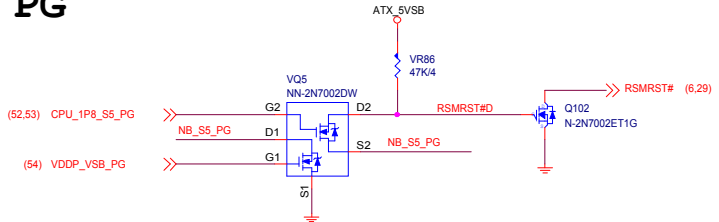
S0 PG



VRM\_Enable circuit



S5 PG



# DDR4\_1.2V@26.2A

15.5A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

Rocpset:4.32K

OCP=Rocpset\*Rdson(Low side)/10uA

=8.2K\*10uA/4mohm

=20.5A

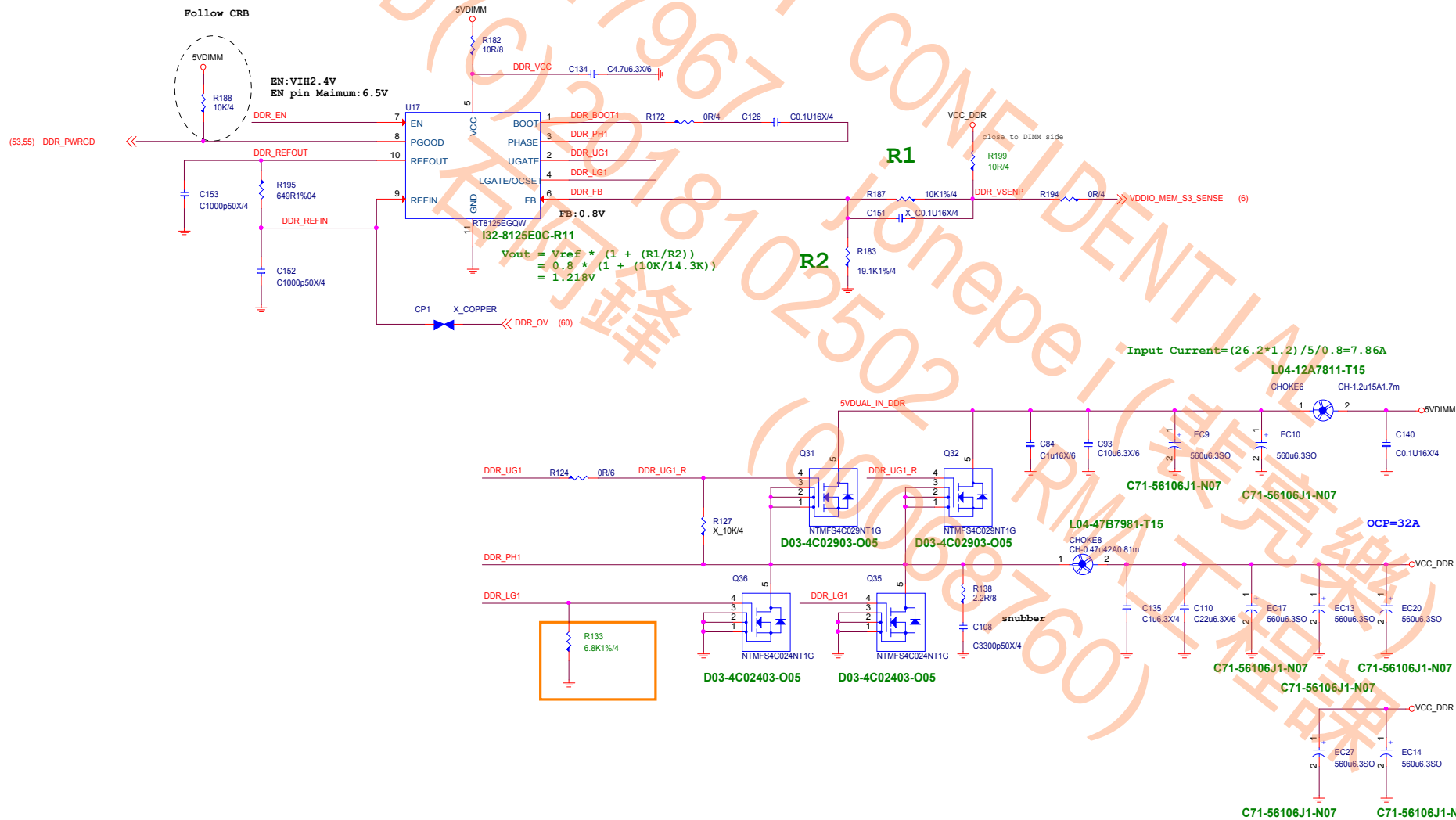
(6,54,55,62) APU\_AMMR1 >> D18 <- S-LRB520S-40T1G DDR\_EN

(29) SIO\_VDDQ\_EN >> R198 <- 0R/4 DDR\_EN 3.12V

EN: VIH2.4V  
EN pin Maximum: 5.5V, RECOMMENDED: 3.6V

Follow CRB

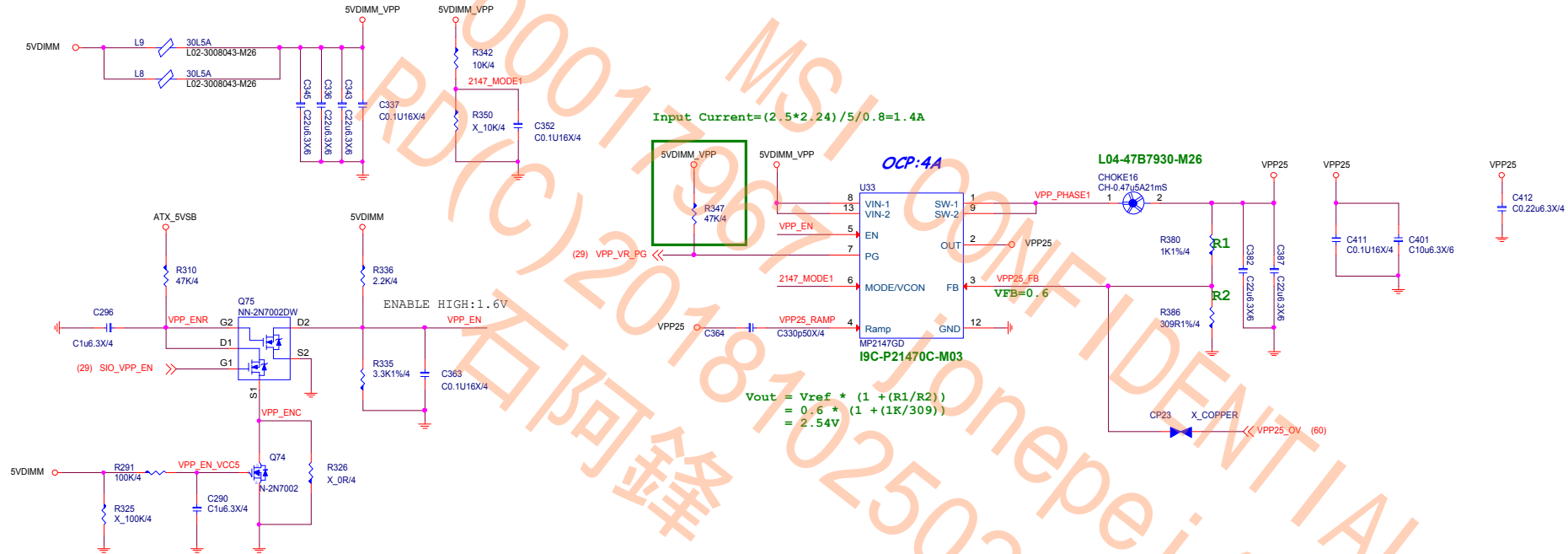
EN: VIH2.4V  
EN pin Maximum: 6.5V





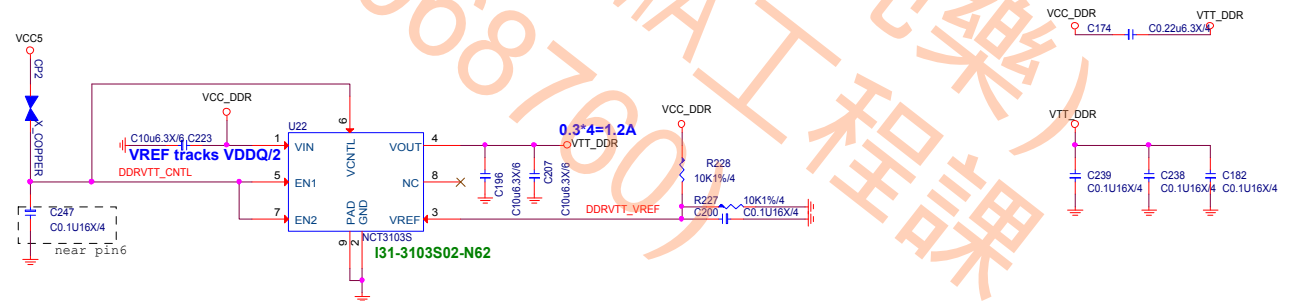
# 4DIMM : VPP25

2.5V@2.24A



## DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils

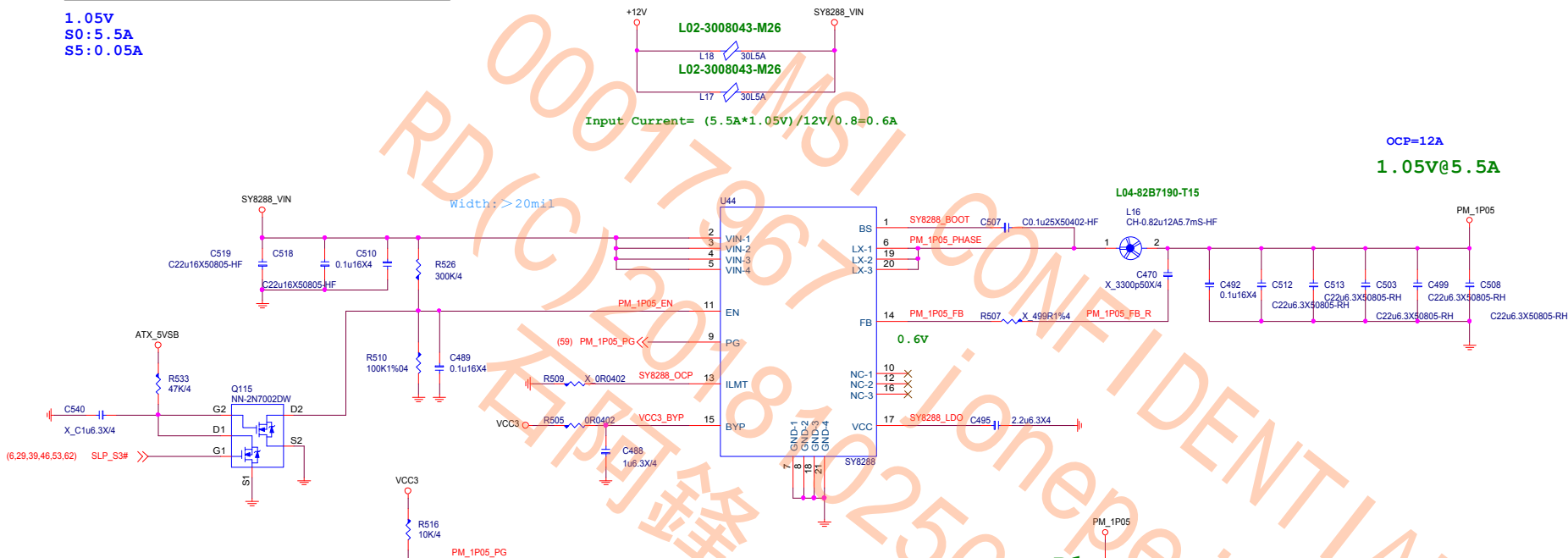


## FOR Promontory 1.05V\_S0

1.05V  
S0: 5.5A  
S5: 0.05A

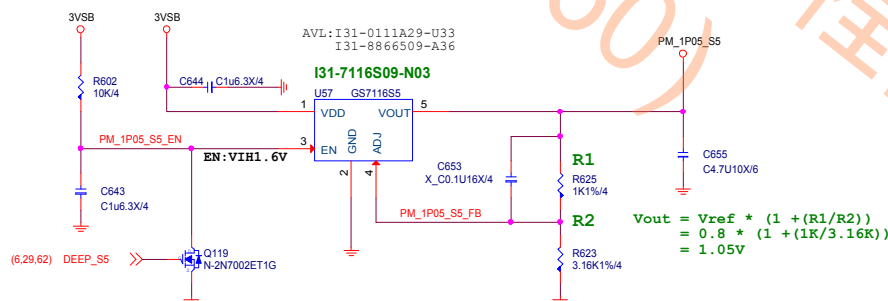
$$\text{Input Current} = (5.5A \times 1.05V) / 12V / 0.8 = 0.6A$$

OCP=12A  
1.05V@5.5A



## FOR Promontory 1.05V\_S5

1.05V@0.05A



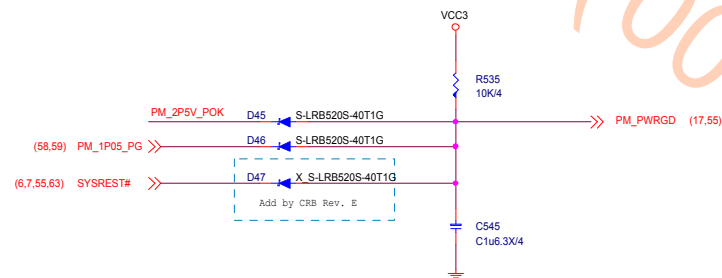
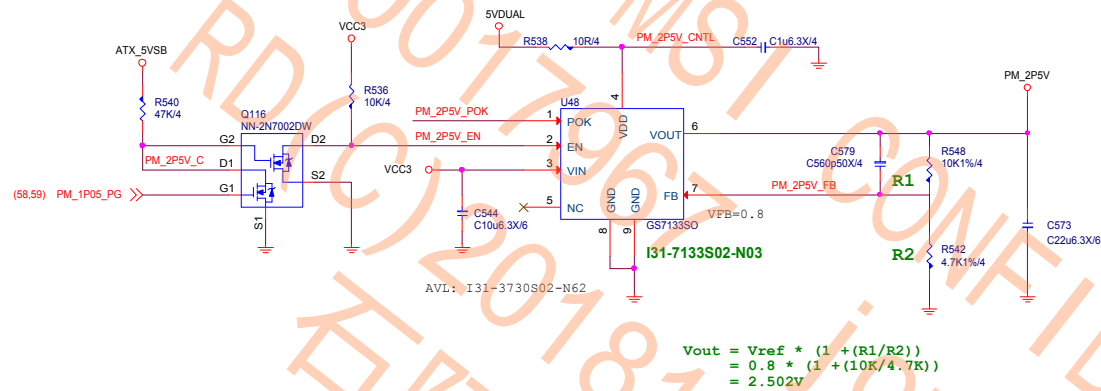
MICRO-STAR INT'L CO.,LTD

MS-7B78

Size	Document Description	Rev
Custom	PROM - SY8288RAC / 1.05V	10
Date:	Tuesday, January 09, 2018	Sheet 58 of 77

## Promontory-2.5V

2.5V@900mA

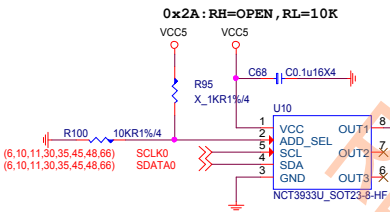


MICRO-STAR INT'L CO.,LTD

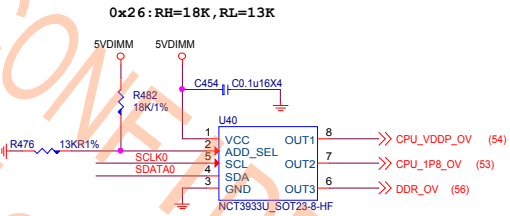
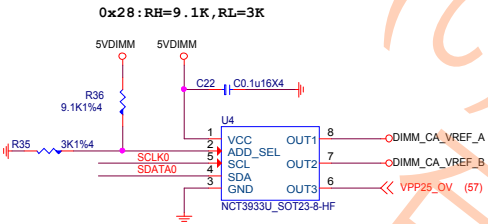
MS-7B78

Size	Document Description	Rev
Custom	PROM - GS7133 / 2.5V	10
Date:	Tuesday, January 09, 2018	Sheet 59 of 77

Over Voltage Control IC



UPI VOLTAGE CONSOLE						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

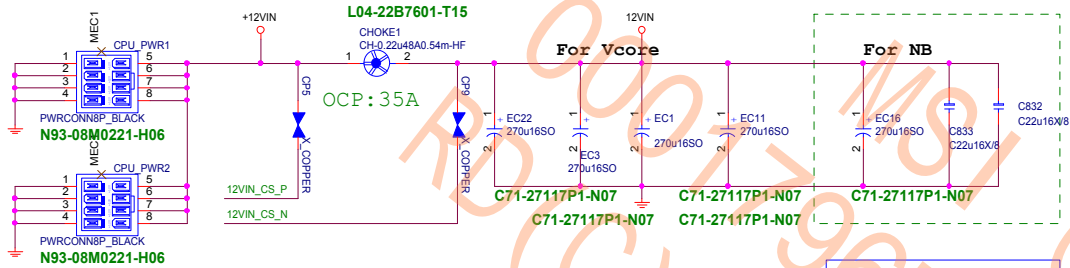


UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



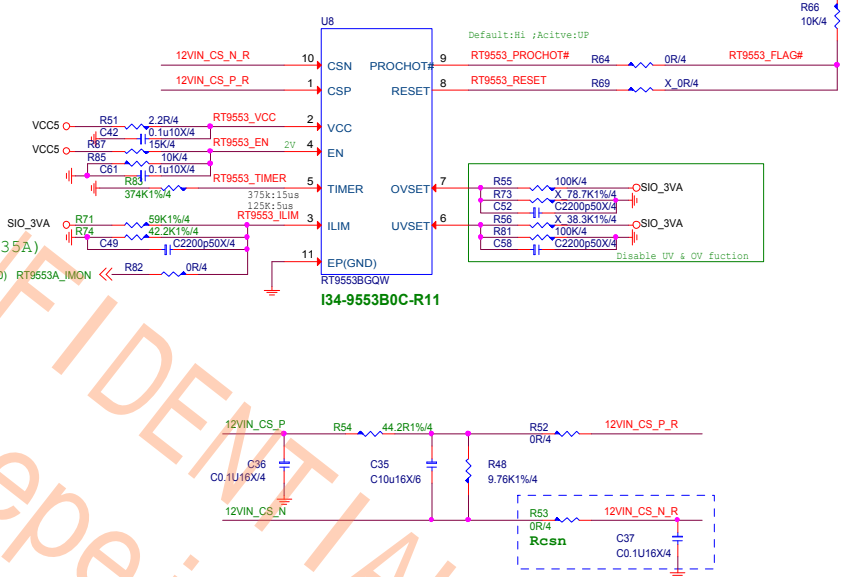
CPU POWER CONNECTOR



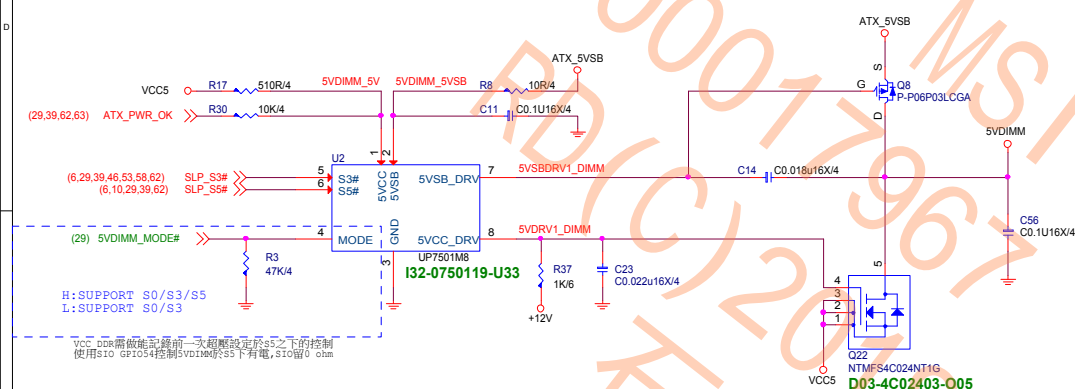
NB		VCCP	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	-> input voltage	Vin = 12	-> input voltage
Vout = 1.4	-> output Vcore	Vout = 1.4	-> output Vcore
D = 0.116667		D = 0.116667	
I <sub>o</sub> = I <sub>coremax</sub> *0.8		I <sub>o</sub> = I <sub>coremax</sub> *0.8	
I <sub>core(max)</sub> = 75	-> Vcore current	I <sub>core(max)</sub> = 125	-> Vcore current
I <sub>avg</sub> = 75	A	I <sub>avg</sub> = 125	A
I <sub>ripple</sub> = [I <sub>o</sub> *√D*√(1-D)] / Phase		I <sub>ripple</sub> = [I <sub>o</sub> *√D*√(1-D)] / Phase	
Phase = 2	-> phase	Phase = 4	-> phase
I <sub>ripple</sub> = 12.03835	A	I <sub>ripple</sub> = 10.03196	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I <sub>ripple(cap)</sub> = 5000m A		I <sub>ripple(cap)</sub> = 5000m A	
COE <sub>TEMP</sub> = 1		COE <sub>TEMP</sub> = 1	
Input Cap. = 3	pcs.	Input Cap. = 3	pcs.

RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



## 5VDIMM FOR DDR



### 3VSB cost down

3.3V@2.63A

**1.05V@0.05A**

VDDBT\_RTC G@4.5uA

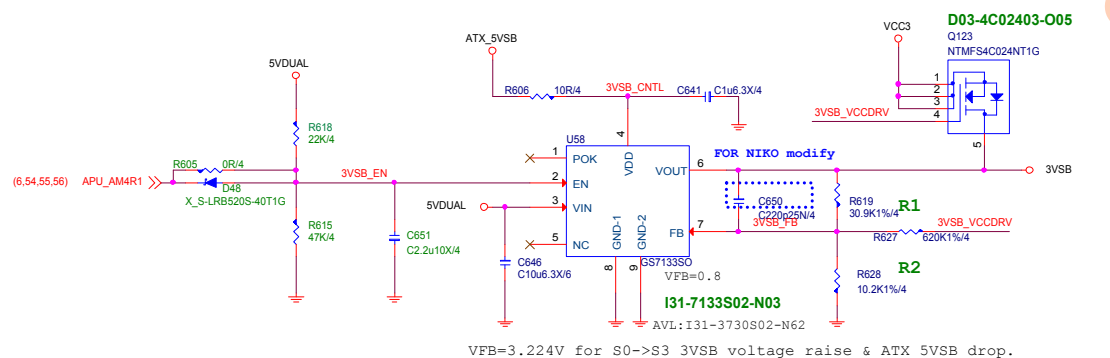
*FCH@0.07A*

CPU@0.25A

PCI @0.75A

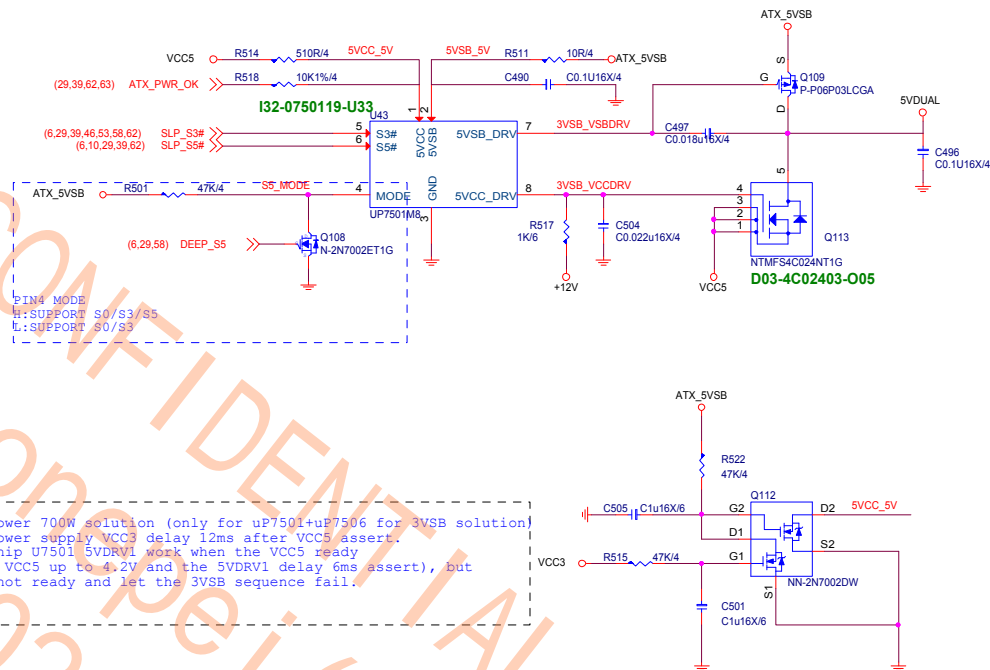
PCIE\*4 @1.5A

USB TYPE-C @0.9mA



$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (30.9K/10.2K)) \\ &= 3.22V \end{aligned}$$

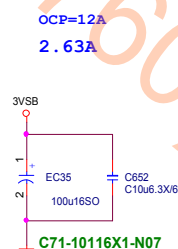
## 5VDUAL For 3VSB、CPU 1.8V、VDDP



```

| For power 700W solution (only for uP7501+uP7506 for 3VSB solution
| The power supply VCC3 delay 12ms after VCC5 assert.
| The chip U7501 5VDRV1 work when the VCC5 ready
| (When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
| VCC3 not ready and let the 3VSB sequence fail.

```



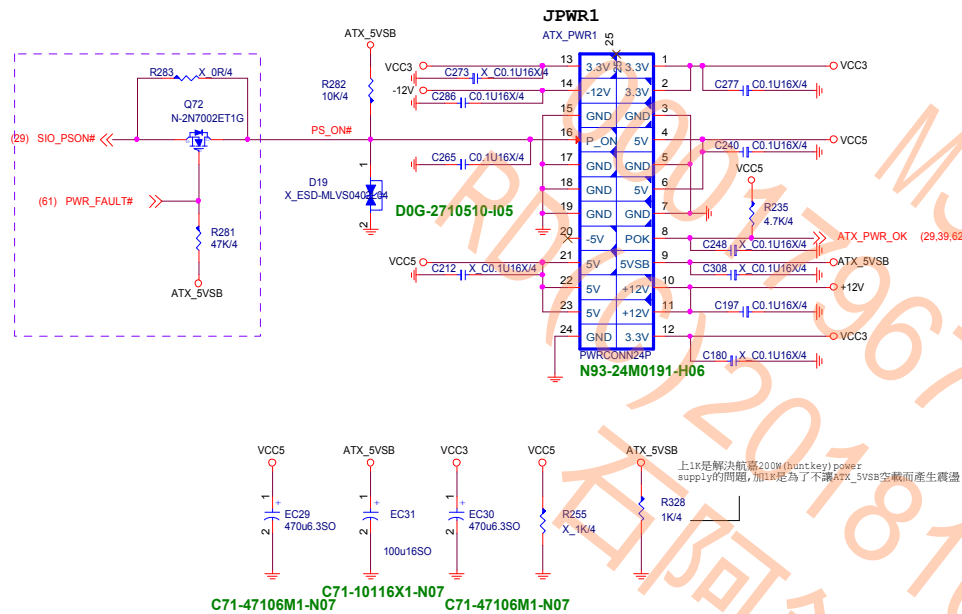
**MICRO-STAR INT'L CO.,LTD**

**MS-7B78**

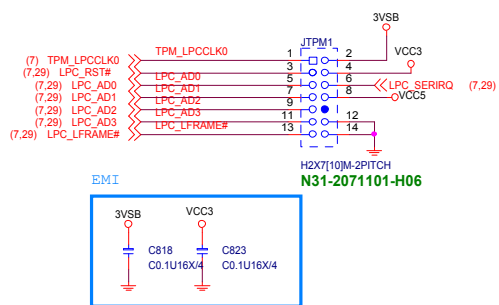
Size Custom	Document Description <b>ACPI - 5VDIMM / 3VSB</b>	Rev 10
Date: Tuesday, January 09, 2018		Sheet 62 of 77



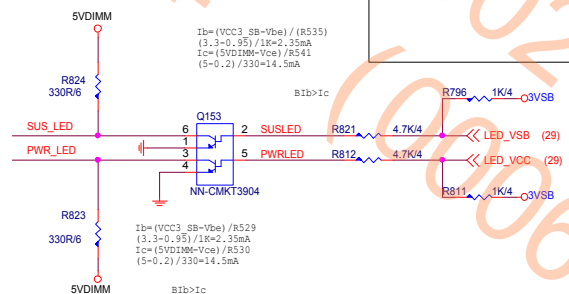
## ATX POWER CONNECTOR



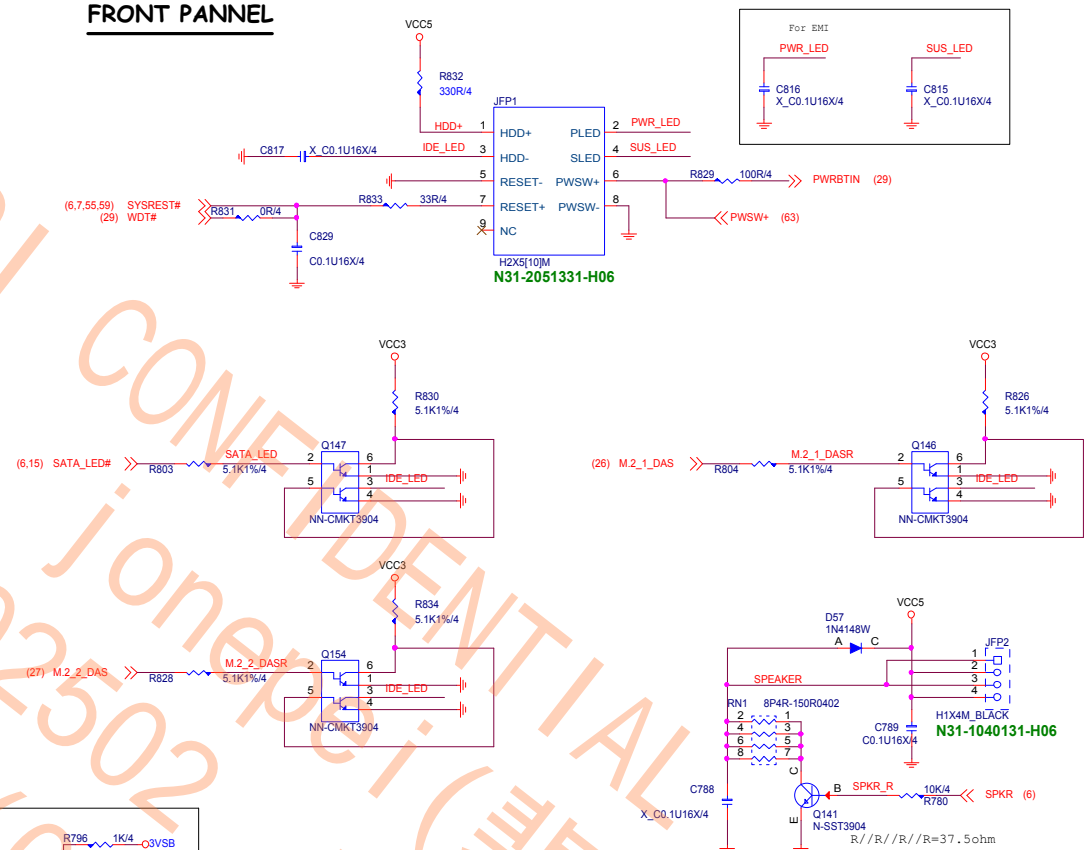
**TPM**



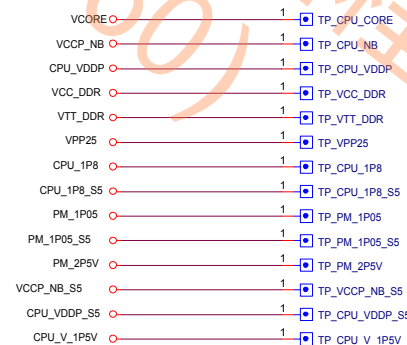
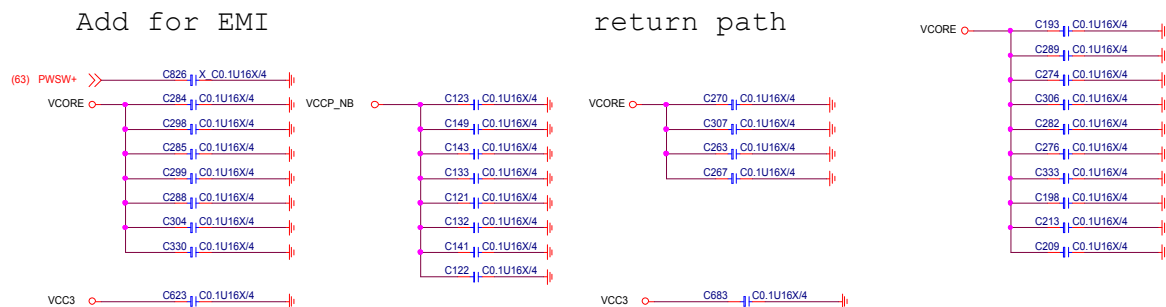
LED ( for NCT6793D)



## FRONT PANNEL



### Voltage Measure Point



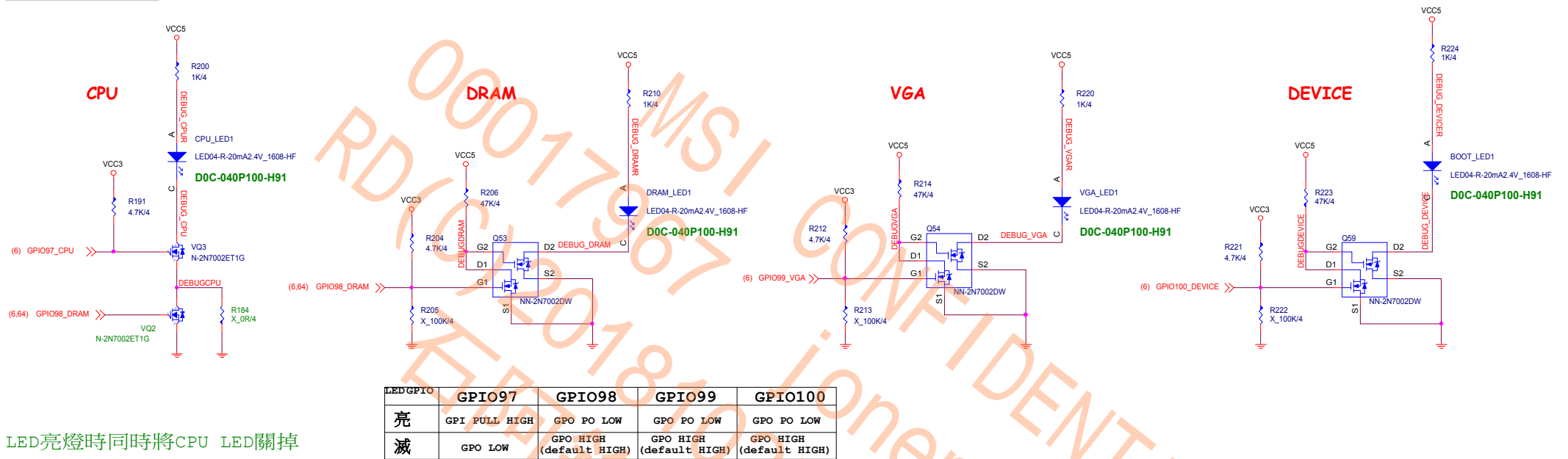
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MS-7B78

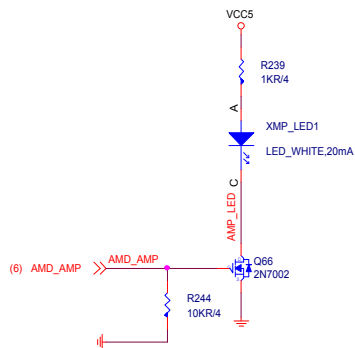
Size	Document Description
Custom	<b>ATX power - FrontPanel / EMI</b>

Date: Tuesday, January 09, 2018 Sheet 63 of 77

## EZ Debug LED

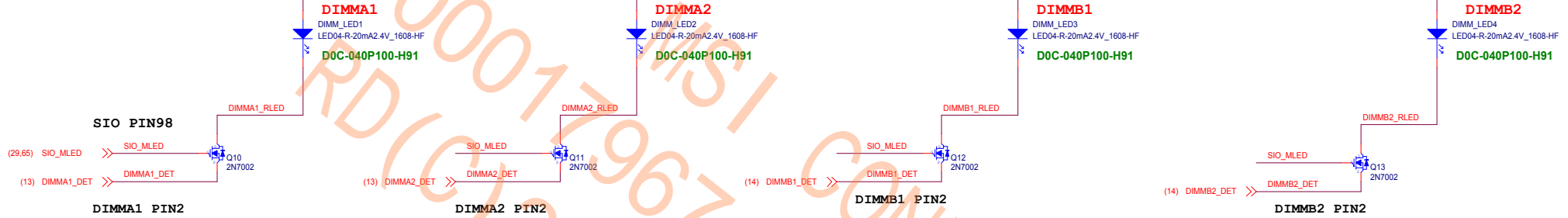


## AMD AMP Detect LED

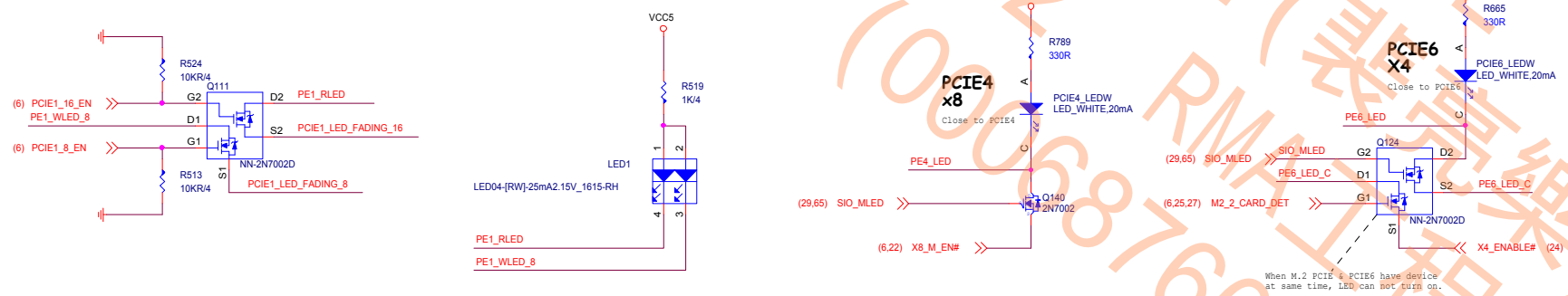


**DIMM\_SLOT      FORM SIO**

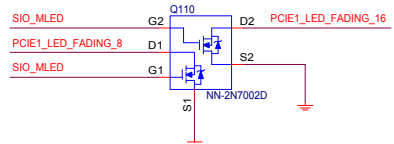
D0C-040P100-H91/D0C-040S500-E07



**PCIE\_SLOT LED      FORM SIO**



	x16	x8	x4
PCIE1	Red	X	X
PCIE1	X	White	X
PCIE4	X	White	X
PCIE6	X	X	White

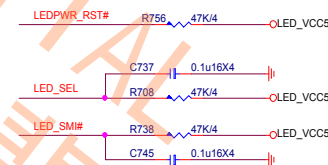
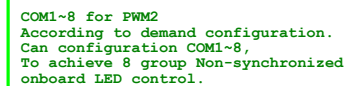


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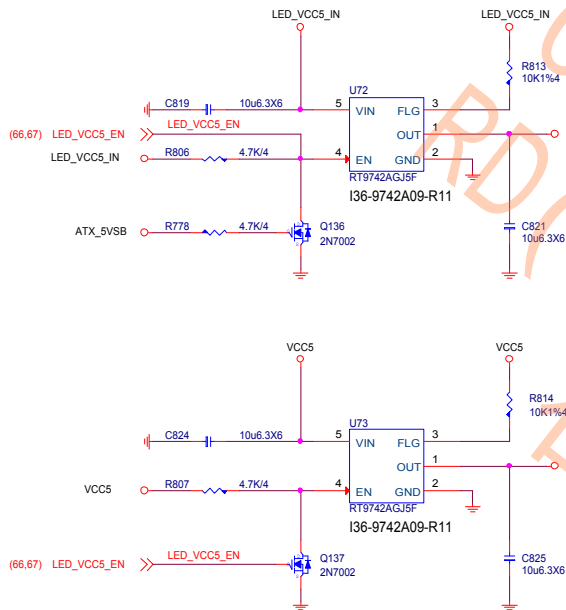
Size Custom	Document Description <b>LED - DIMM / PCIE SLOT</b>	Rev 10
Date: Tuesday, January 09, 2018	Sheet 65 of 77	

C345 & C359 near VDD Pin.

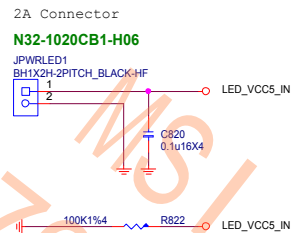


~~If SPEC has LED demo function without demo button, DEMO\_DET# must pull up to LED\_VCC5 and control by LED\_VCC5\_EN. PS. R1000 remove, R1457 and Q296 need to stuff~~

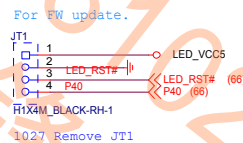
## EXTERNAL POWER INPUT



## External Power



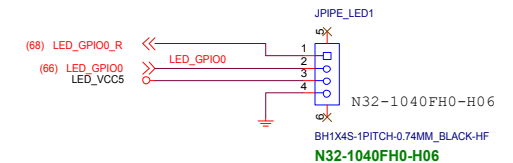
## JT1 for FW update



## LED Demo Button

1 PCH HEATSINK LED  
PCS LED\*0.16W=W

2 AUDIO/IO Cover LED  
PCS LED\*0.16W=W



3 MOS HEATSINK LED  
PCS LED\*0.16W=W

JPIPE\_LED3 no SPEC

JPIPE:PIN1:output ,PIN2:input

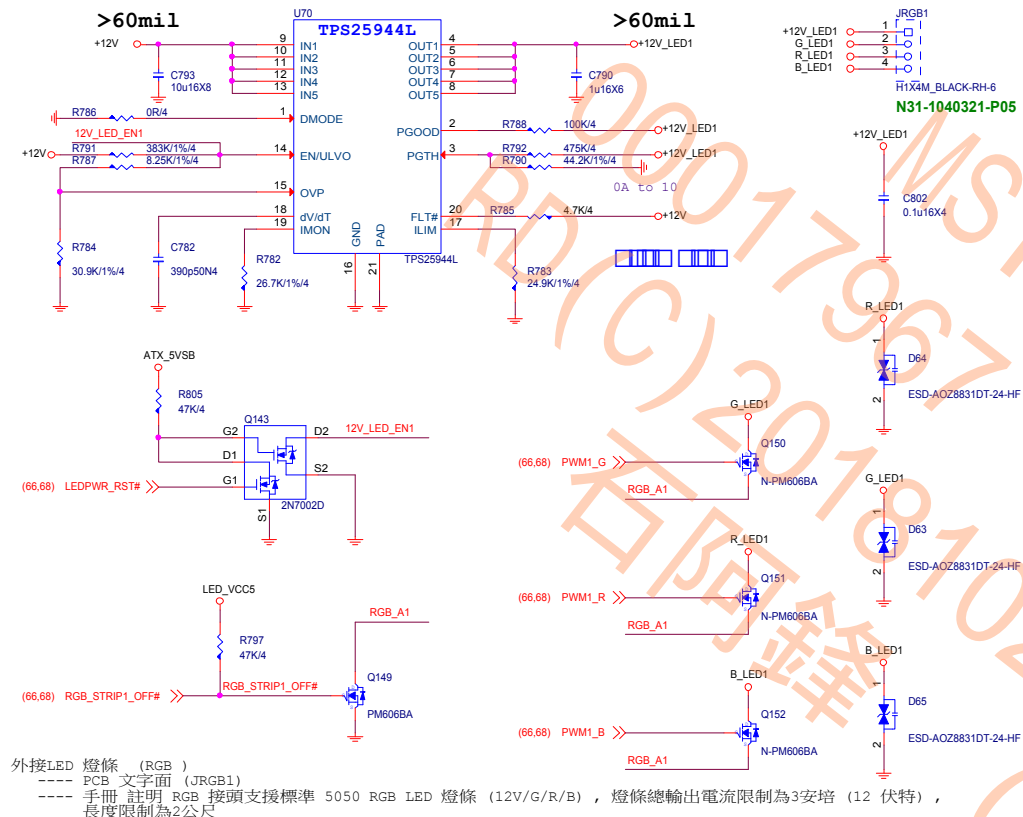
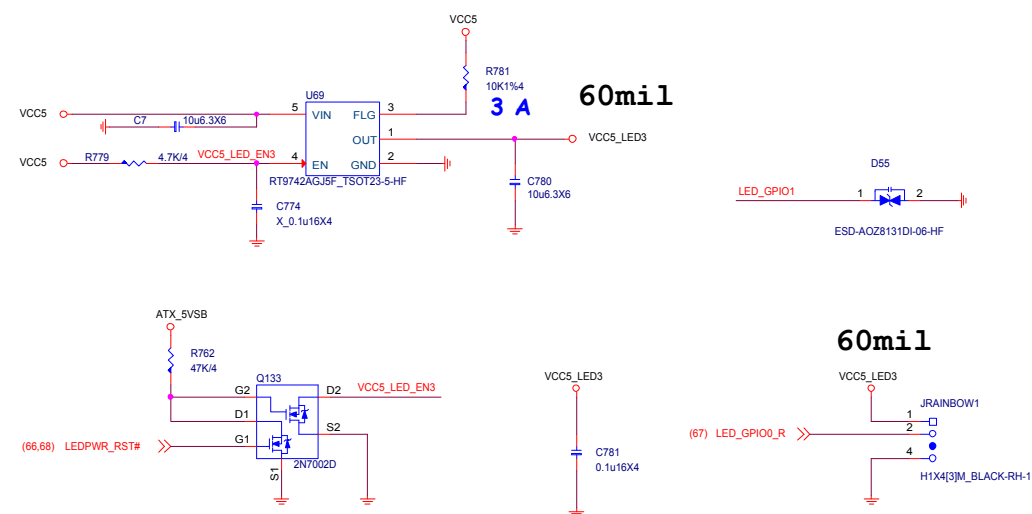


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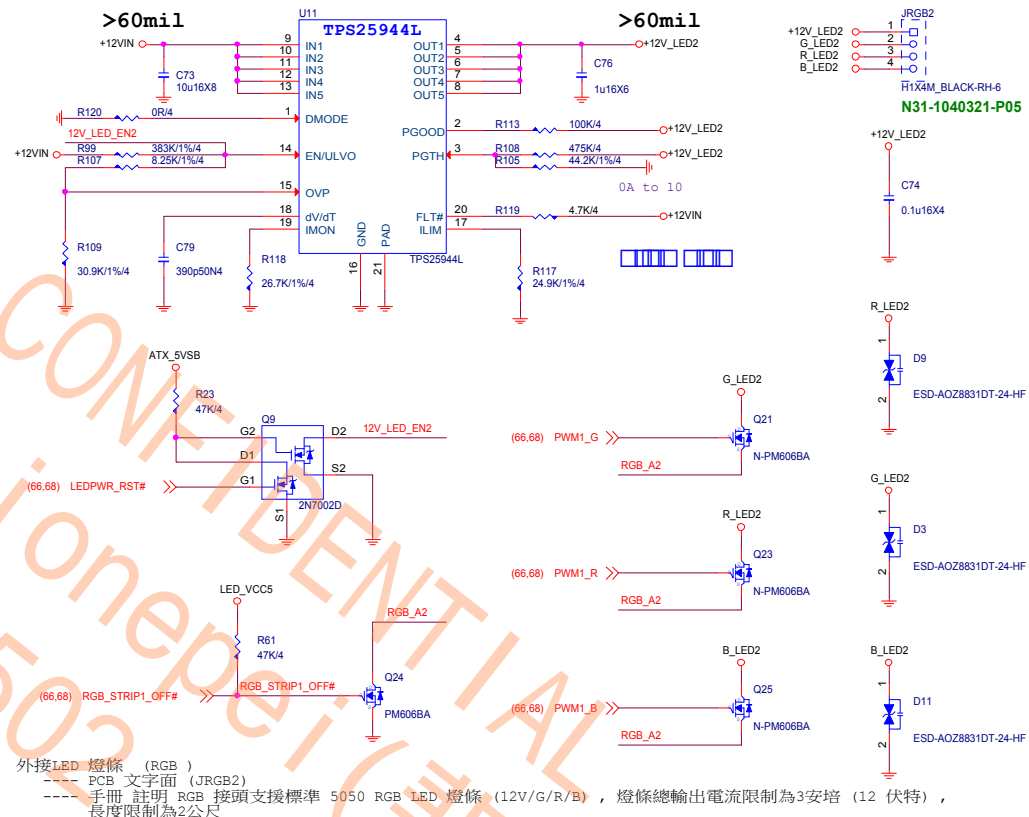
MS-7B78

Size	Document Description	Rev
Custom	LED - Power / JPIPE	10
Date:	Tuesday, January 09, 2018	Sheet 67 of 77

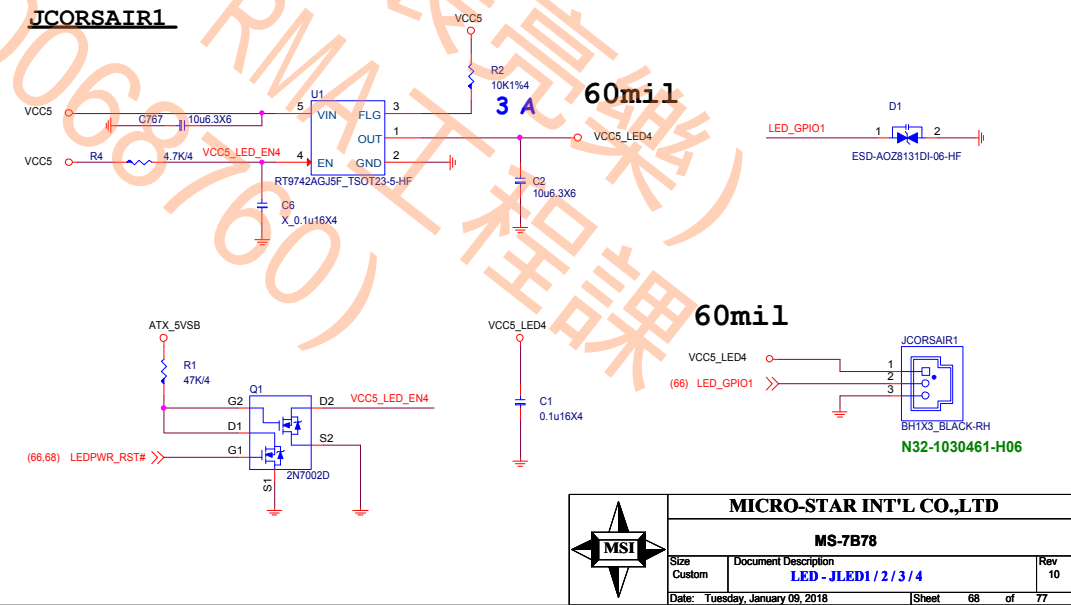
## JRGB1

JRAINBOW1

## JRGB2



JCORSAIR1



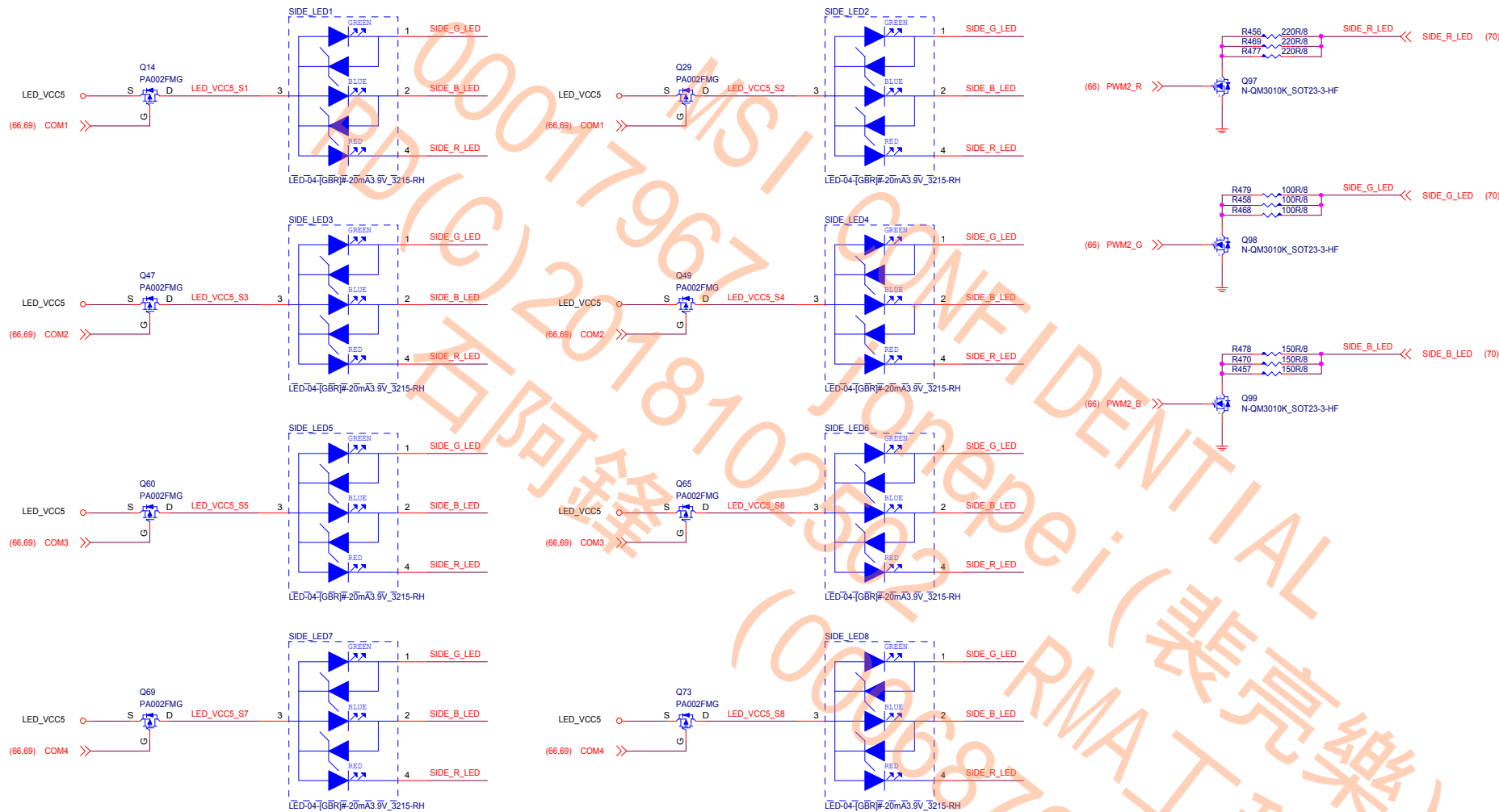
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**MS-7B78**

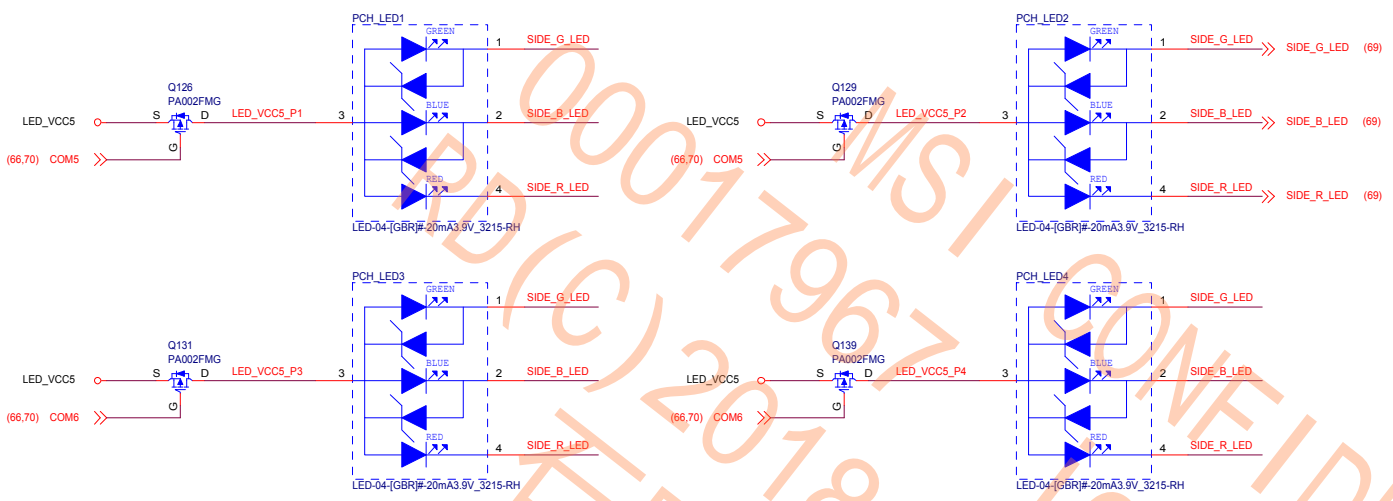
Size Custom	Document Description <b>LED - JLED1/2/3/4</b>	Rev 10
Date: Tuesday, January 09, 2018		Sheet 68 of 77



# Right Track LED \*8



PCH LED \*4



MSI CONFIDENTIAL  
00017967 jonepei (裴亮樂)  
RD(C)2018102502 RMA工程課  
石阿鋒 (00068760)



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MS-7B78

Size Custom	Document Description <b>BOM Option</b>	Rev 10
Date: Monday, January 08, 2018		Sheet 71 of 77

## CPU Socket



E95-0000021-C22

E95-0000022-C22

## PCB

PCB



7B78\_10

PD0-07B4520-G37

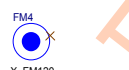
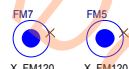
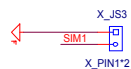
PD0-07B4520-E48

## MOS HEATSINK

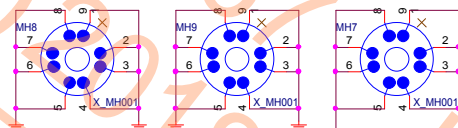
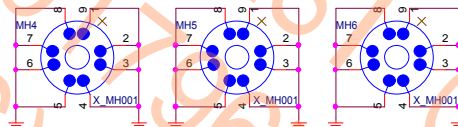
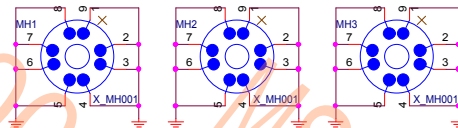
IO COVER+MOSA

mos heatsink

## Simulation



## Optics Orientation Holes



## MANUAL PART

UEFI1  
G51-M1SPXXA-A09  
G51-M1SPXXA-A09

HDMI\_LA1  
Label  
HDMI  
HDMI LABEL  
Y01-RHDMI03-000



BAT1\_X1  
BAT-BCR2032P

AVL1:  
D06-0100101-F52  
D06-0100101-K26



X470

CFOS  
Y02-MU00170-CFO  
Y02-MU00170-CFO

NAHIMIC  
Y02-MU00100-NAH  
Y02-MU00100-NAH

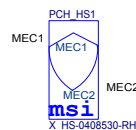
SLI  
Y01-RNVIDIL-000  
Y01-RNVIDIL-000

SSE1  
WIFI  
604-4442-020

XSPILT  
X\_Y02-MA00401-XSP  
Y02-MA00401-XSP

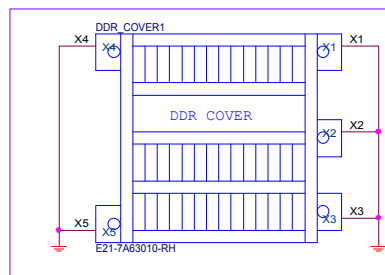
SSE  
X\_Y02-MA00101-SSE  
Y02-MA00101-SSE

## PCH HEATSINK



PCH Heatsink

## DDR COVER



0901 Modify DDR\_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

## Audio COVER



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MS-7B78

Size	Document Description	Rev
Custom	Manual Parts	10
Date:	Tuesday, January 09, 2018	Sheet 72 of 77